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Delta modulation incorporating integrated circuits : a feasibility study.

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DELTA MODULATION INCORPORATING INTEGRATED CIRCUITS; A FEASIBILITY STUDY

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THESIS

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by

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by

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ABSTRACT

Pulse-modulation and integrated circuits, respectively, are the most recent major advances in the communications field and in electronic devices. The evolutionary development of one pulse-modulation technique, Delta Modulation, is examined in this thesis to determine the feasibility of extending its evolution to the inclusion of integrated circuits in its design. An experimental circuit, demonstrating this feasibility, is described and evaluated.

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I. INTRODUCTION

The increasing demands for communications systems capable of handling large volumes of traffic have forced the development of new communications techniques. This need has been met, in part, by the advent of pulse-modulation and multiplex systems. The devices required to implement these communications techniques have also evolved through the years from vacuum tubes to transistors and integrated circuits.

This thesis considers one pulse-modulation technique---delta modulation. Chapters II through IV, based upon published papers, present the development of delta modulation (DM) through the time when discrete transistors were used. To extend the evolution to integrated circuits, an experimental circuit incorporating these newest devices has been designed and built. Tests upon this system demonstrated satisfactorily the ability to transmit sinusoidal and triangular waveforms.

Chapter II describes the various types of pulse modulation and compares briefly delta modulation and pulse-code modulation. A detailed description of delta modulation follows in the third chapter of this thesis. The theoretical origin of DM is described and typical circuit waveforms are presented for each of three types of feedback methods.

The fourth chapter illustrates, by representative circuits, the implementation of the DM theory into experimental

test systems. Incorporation of transistors and the application of DM in voice-transmission and telemetry systems is also presented. The latter part of the chapter discusses a major modification of conventional DM known as Delta-Sigma Modulation.

The remaining chapters describe the design, construction and testing of a DM system incorporating integrated circuits. The operation of each functional portion of the circuit is described. The objective of this test circuit is to demonstrate the feasibility of the integrated circuitry in DM. As a consequence, the results are limited in scope, but comparison with earlier systems will be made where possible.

II. PULSE MODULATION

For many years, communications relied upon continuous transmission of information signals. These systems used the familiar amplitude, frequency and phase modulation techniques. The proposal of pulse modulation, therefore, was a radical change in information-handling techniques.

Pulse modulation was based upon the sampling principle which stated that any sine wave could be reproduced if its amplitude was known at each of two equally spaced time intervals of each cycle. Since only a small fraction of each cycle was required to transmit all the information about that channel, it was proposed that several channels could be interlaced, with resultant reduction of the total number of channels. This interlacing technique is known as multiplexing (8).

Several forms of pulse modulation have been proposed. These are:

A. Pulse-amplitude modulation (PAM)---in which the amplitude of successive pulses is determined by the amplitude of the sampled signal at the instant of sampling.

B. Pulse-frequency modulation (PFM)---in which the instantaneous pulse repetition frequency is determined by the value of the sampled signal at the time of sampling.

C. Pulse-position modulation (PPM)---in which the position, in time, of the leading edge of a pulse is varied about some reference position depending upon the amplitude of the sampled signal at the time of sampling.

D. Pulse-width modulation (PWM)---or pulse-duration modulation (PDM)---in which the width of the pulse is varied about some reference width depending upon the magnitude of the sampled signal at the time of sampling.

E. Pulse-code modulation (PCM)---in PCM, the amplitude of the signal is quantized into 2^n distinct levels which are numbered 0, 1, 2,.....2^{n-1}. The number of the level into which the amplitude of the signal falls at the time of sampling is converted into binary form. In transmission, a pulse is sent whenever a one occurs, and no pulse, or a pulse of opposite polarity is sent whenever a zero occurs. Therefore, for each sample, a series of n pulses will be transmitted of magnitude one or zero.

In all of the above methods except PCM, the receiver must perform two functions: 1) it must detect the presence of the pulse, and 2) it must determine some unique characteristics of the pulse such as its amplitude, position, duration or frequency. The presence of noise in the transmission can affect the value of these characteristics.

In PCM, however, the only requirement of the receiver is to determine the presence or absence of the pulse. In this system, reliable communications can be maintained with a signal-to-noise ratio as small as 2 (2).

The largest drawback to PCM is the complexity of the analog-to-digital and digital-to-analog converters. Another pulse modulation system has been developed to avoid this complexity, and it is known as delta modulation. This system enjoys many of the advantages of PCM, including the capability of transmission with small signal-to-noise ratios. In addition, its simplicity and low cost can meet requirements that PCM can satisfy only with complexity and accompanying higher cost. The major disadvantage of DM is the larger bandwidth required.

Many authors have compared DM with PCM. Zetterberg (38) published a paper in 1955 giving an outstanding comparison from the information theory point of view. Most of the references cited in this thesis have at least one section concerning DM and PCM advantages. References not cited, but which have good theoretical comparisons, include Abate (1), Bowers (5) and O'Neal (30).

In the remainder of this thesis, only delta modulation will be considered. Emphasis will be placed upon the evolution of DM into a system incorporating integrated circuits.

III. DESCRIPTION OF DELTA MODULATION

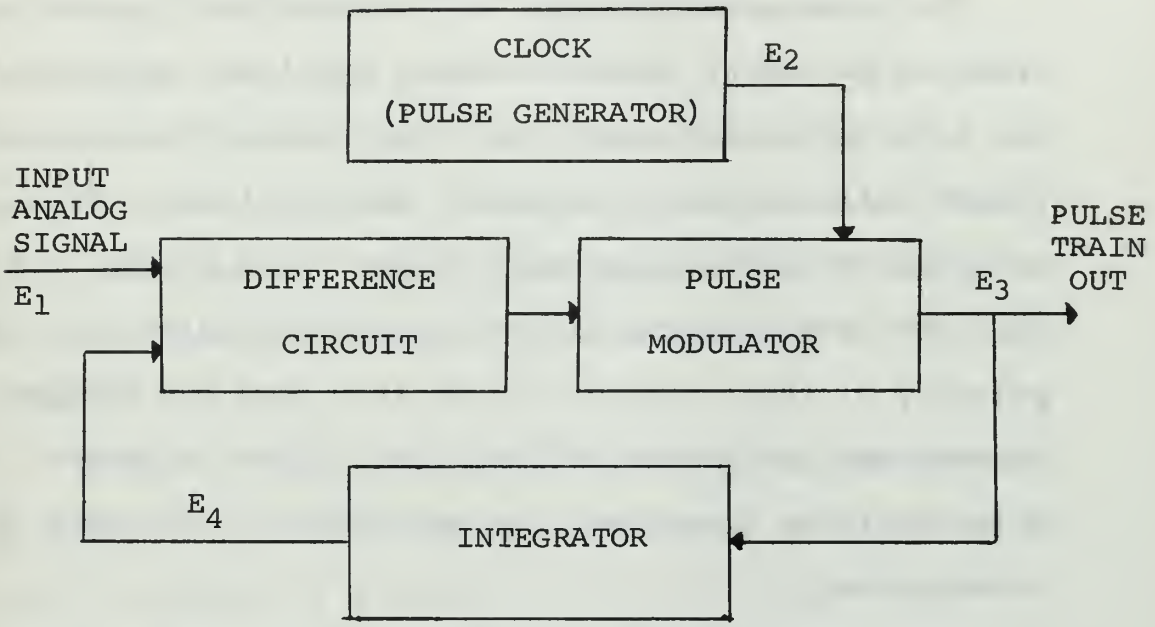
The basic delta-modulation system provides a means of encoding analog signals in communications and control systems. The transmitted signal, consisting of pulses, represents binary decisions which are determined by the polarity of the difference between the modulating signal and an approximation of this signal.

This method was first described in a 1946 French patent by E. M. Deloraine, S. Van Mierlo and B. Derjavitch (10). The first papers published describing the theory of delta modulation made their appearance in 1952 (7, 32). One of these, by F. de Jager, entitled "Delta Modulation, A Method of P. C. M. Transmission Using the 1-Unit Code" (7), forms the theoretical basis for much of the succeeding research by others. De Jager's paper presented the basic system, the use of three types of quantized feedback, a description of quantizing noise, and an interpretation of delta modulation in terms of information theory.

A. SYSTEM DESCRIPTION

The block diagram in Figure 1 depicts the basic or conventional delta-modulation system. The input analog signal is fed into a difference circuit or comparator. The function of the comparator is to compare the input with the integrator output. The comparator output will be one of

ENCODER



DECODER

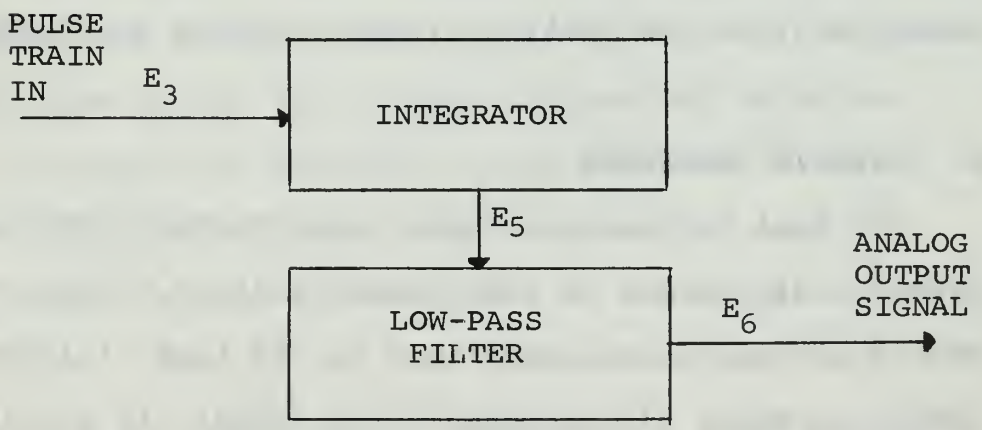


Figure 1: Conventional Delta Modulation

two possible levels; the level chosen (high or low) depending on which of the two inputs is larger.

The pulse generator or clock independently produces a train of pulses of fixed duration, amplitude and period. In the pulse-modulator circuitry, the level of the comparator output will control or determine the modulator output. This modulator output will consist of the clock pulses, but it will now have either positive or negative polarity. The polarity of these pulses will be such that the feedback loop through the integrator reduces the difference between the original input signal and its approximation produced by the integration.

The transmitted train of pulses, consisting of positive and negative pulses, arriving at the decoder are integrated with an integrator identical to that of the encoder. The integrated output is smoothed by the low-pass filter, producing a close realization of the original input signal.

B. CIRCUIT WAVEFORMS

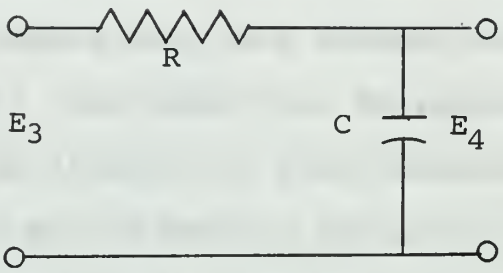
How well the decoder output approximates the input depends, of course, on the characteristics of the system. One of the major considerations is the type of integration used. De Jager (7) proposed three forms: 1) single-integration, 2) double-integration, and 3) double-integration with prediction. The simplest circuits for each of these forms are shown in Figure 2.

1. Single-Integration Feedback

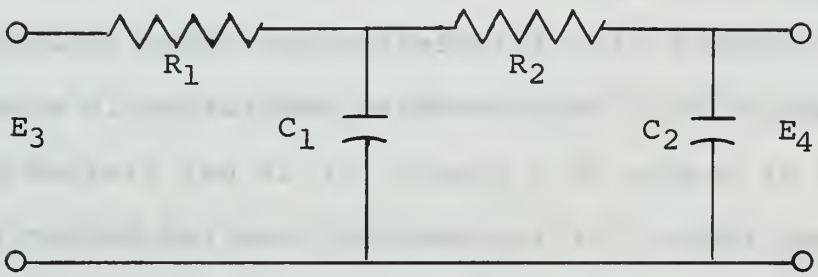
With single-integration, the difference circuit makes a comparison between the input signal and the staircase-like output of the integrator. (See Figure 3.) The difference between these two signals is known as quantizing noise, or noise created in the system by the quantization process. Statistical analysis of this quantizing noise has been examined in detail by Van de Weg (35), and O'Neal (29, 31).

Figure 3 also illustrates two other limitations of delta modulation. Because delta modulation is a measure of the rate of change of a signal, it is not limited by the signal amplitude. It is, however, limited by the rate of change of amplitude which it can follow (encode). This limitation, known as slope-limiting, is illustrated in Figure 3 by region A. In this region the input signal rises too rapidly for the staircase signal to follow. The resulting magnitude of the signal, E_6, is observed to be too small. To reduce or eliminate slope-limiting, a higher clock frequency or a larger step size must be used.

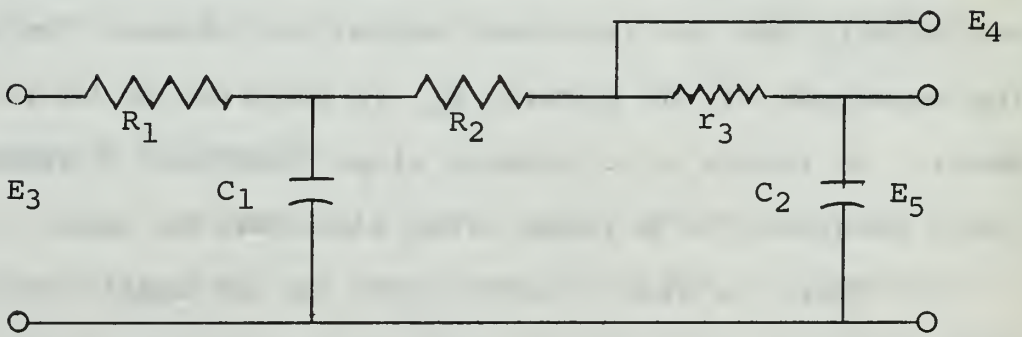
There is also a lower limit on the amplitude of the input signal. This occurs when the peak-to-peak amplitude is less than the magnitude of each step in the integrator output. The modulator output will, as a result, consist of a sequence of pulses alternating in polarity. An example of this occurs at region B in Figure 3.



(a) Single-integration feedback



(b) Double-integration feedback



(c) Double-integration feedback with prediction

Figure 2: Simple Integrating Feedback Circuits

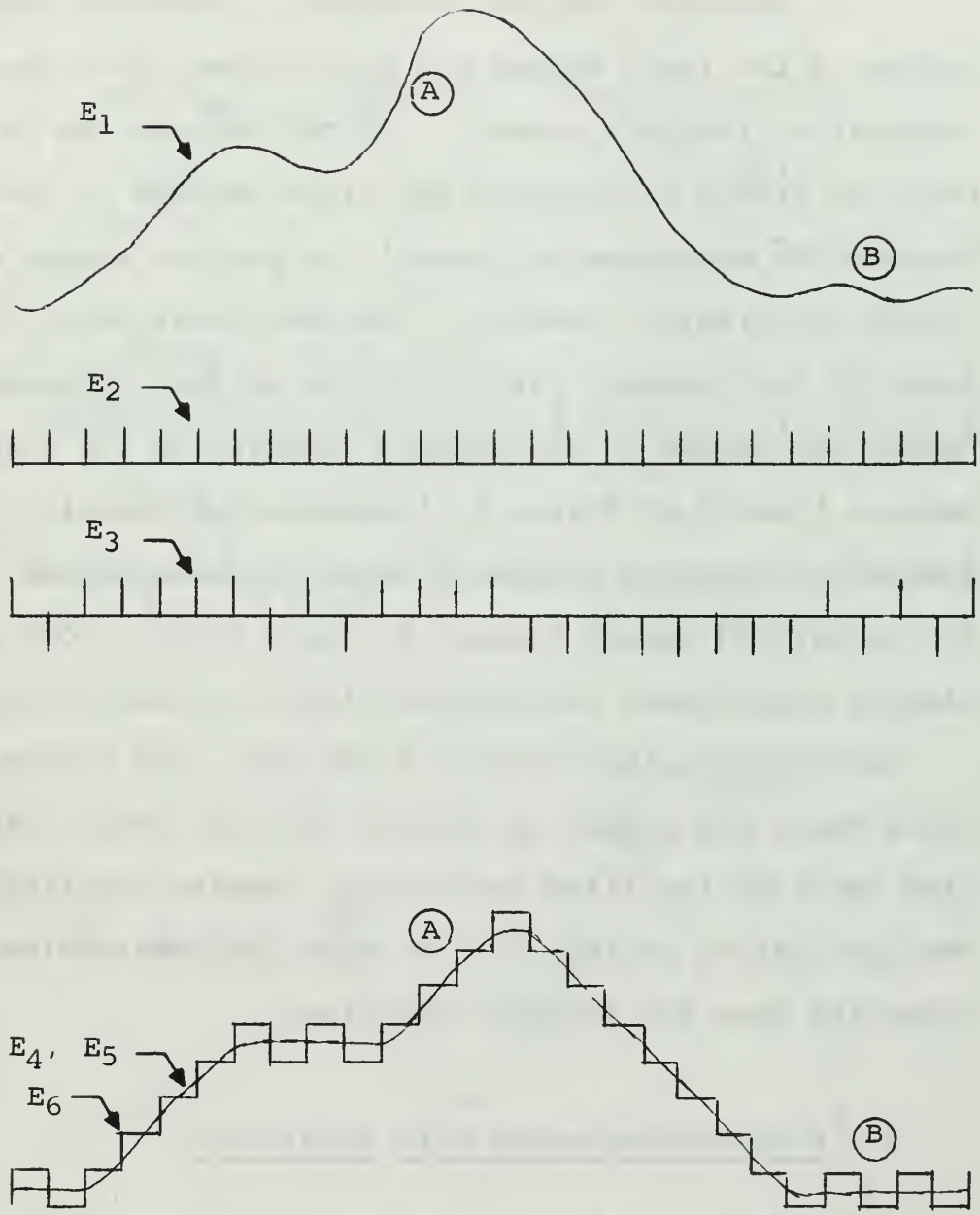


Figure 3: Single-Integration Feedback Waveforms

2. Double-Integration Feedback

A smoother, but not necessarily improved, approximation of the input signal can be obtained using the double-integration feedback network. In this system the pulses have the effect of changing the slope instead of the amplitude of the approximation signal. A problem arises with double integration, however. The additional delay introduced in the feedback circuit by the second integrator causes the system to be somewhat sluggish in its response. Regions A and B of Figure 4 illustrate the inability of the system to sense the change in slope of the original input. The integrated output signal, E_4, as a result, does not closely approximate the applied signal in these regions.

Assuming the input signal to be zero, the situation can arise where the signal E_4 crosses the zero level with a high value of its first derivative, causing oscillations. The oscillatory period can have many different values, depending upon the initial conditions.

3. Double-Integration With Prediction

To eliminate this oscillatory tendency, de Jager (7) proposed the third network in Figure 2. If the difference-circuit input is supplied from a point slightly ahead of the double-integrator output, some prediction capability is introduced. The voltage E_4 now consists of the voltage

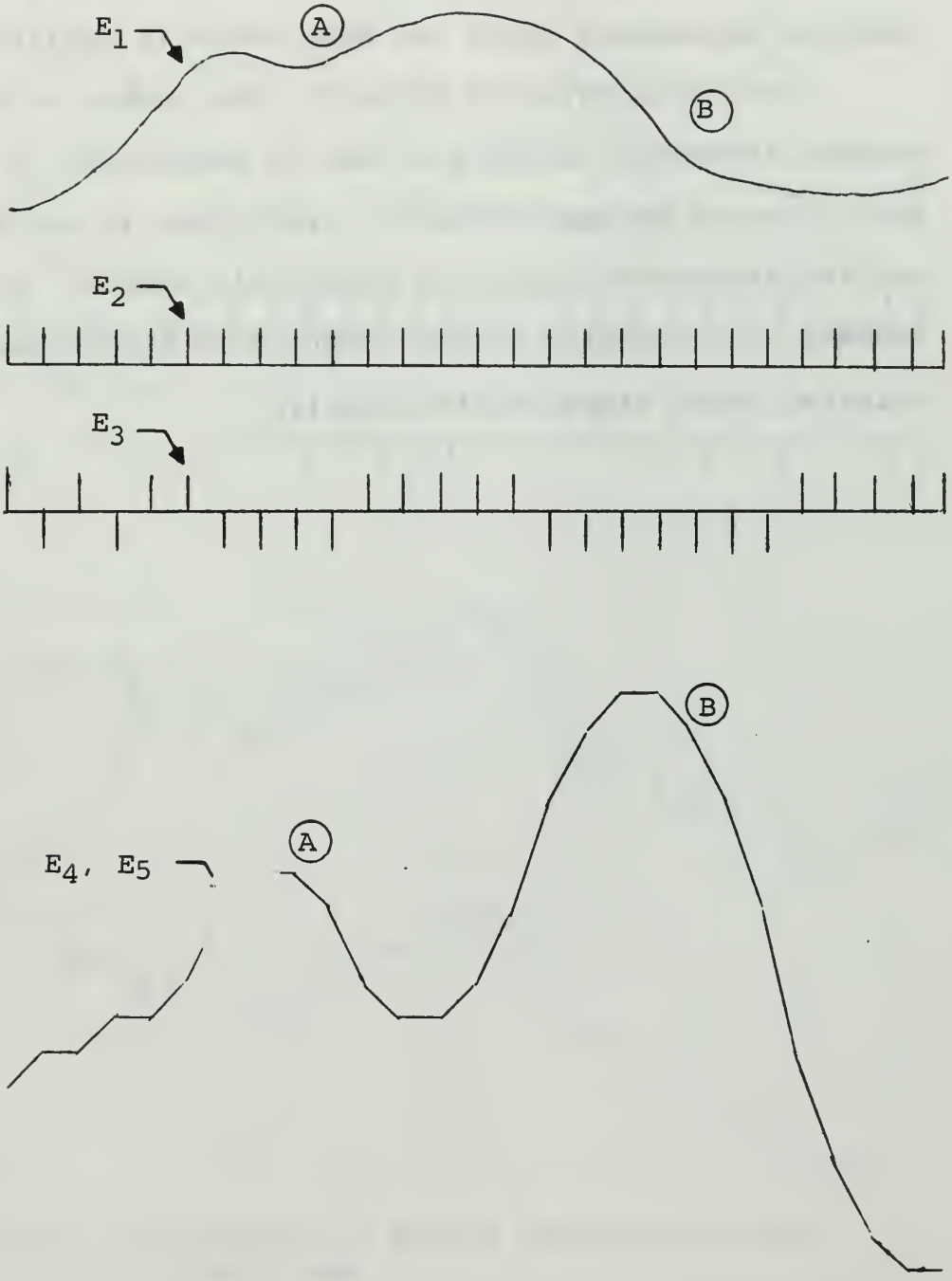


Figure 4: Double-Integration Feedback Waveforms

across C_2 plus the small voltage across R_3. This is a type of predictor circuit, since this output is indicative of the voltage across C_2 at some future time, assuming a constant slope is maintained until the next pulse is applied.

As illustrated in Figure 5, the output of the encoder integrator suffers a loss in smoothness in its wave form. In the decoder, however, prediction is not needed and the integrated output is relatively smooth. In the decoder, the low-pass filter output does approximate the original input signal quite closely.

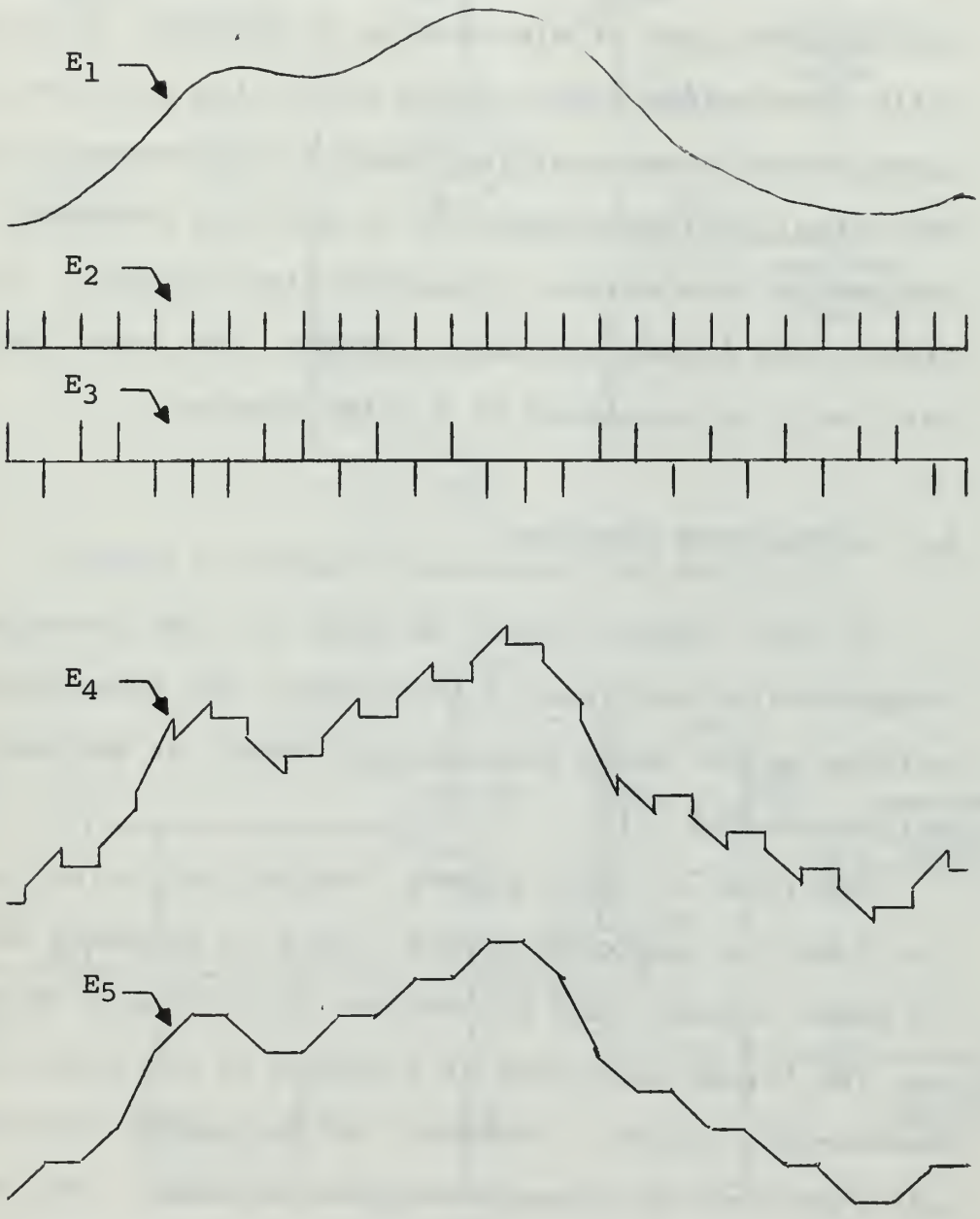


Figure 5: Waveforms for Double Integration with Prediction

IV. CIRCUIT REALIZATIONS

The evolution of delta modulation circuit realizations has followed that of electronics in general. Initially built with vacuum tubes, delta modulation circuits quickly incorporated transistors as these devices were developed. The intent of this chapter is to show the evolution of delta modulation with several representative circuits. Utilization of the latest electronic device, the integrated circuit, will be presented in a later chapter.

A. VACUUM-TUBE CIRCUITS

In 1954, shortly after de Jager (7) had presented his comprehensive analysis of the theory, two theses were written at the Naval Postgraduate School in Monterey, California (24, 2).

The first of these papers, dealing only with the encoding function, proposed several forms of encoders (24). Some of these encoders are illustrated in Figures 6 through 8.

The triode modulator of Figure 6 is the most elementary vacuum-tube encoder. However, as the author indicated, the adjustment of the circuit is quite critical. The unipolarity system tends to either pass or eliminate an excessive number of pulses, the latter condition being more common. In addition, the output amplitude is not constant but varies with the magnitude of the difference signal.

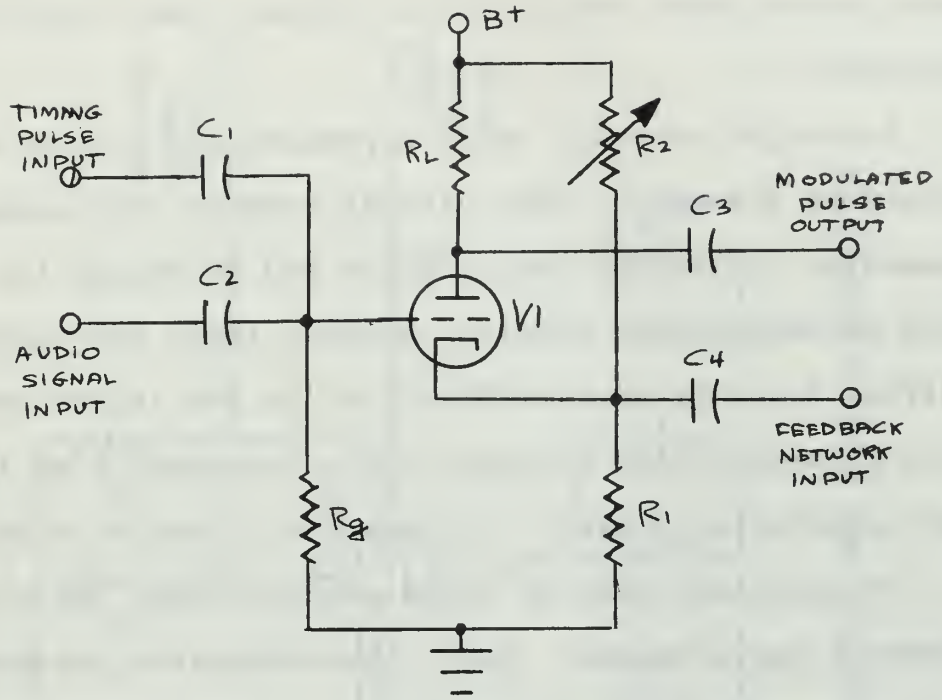


Figure 6: Triode Comparator and Modulator

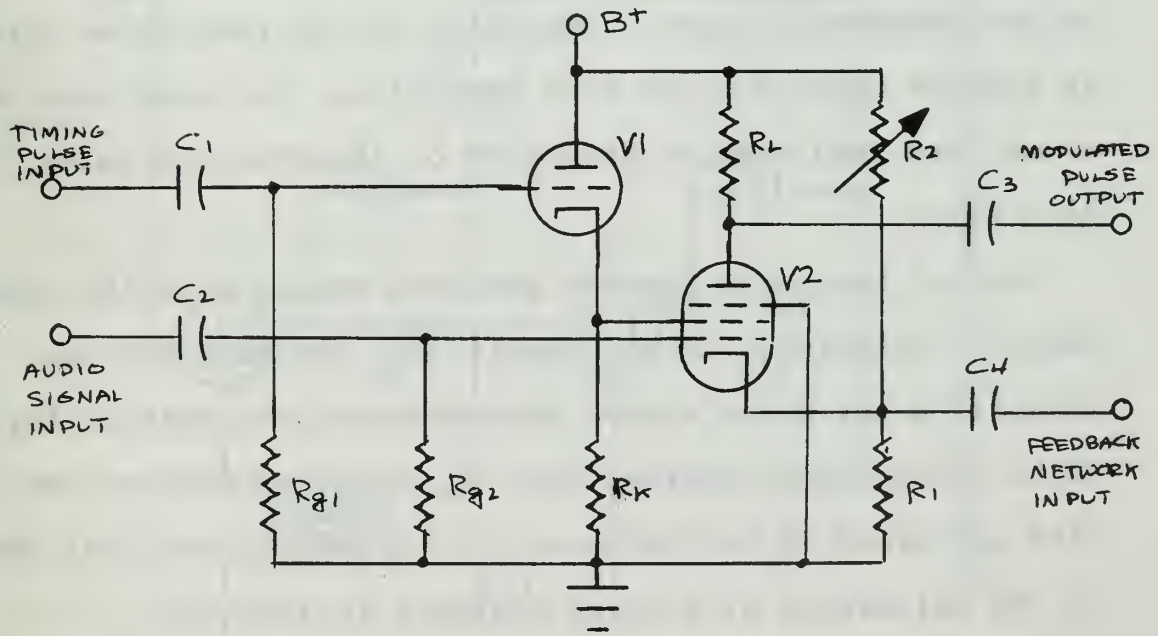


Figure 7: Pentode Comparator and Modulator

This necessitates the use of a limiter stage following the modulator.

A similar circuit, using a pentode and triode is illustrated in Figure 7. This circuit reduces the timing-pulse generator regulation requirements and decreases the likelihood of capacitance coupling between input and output. It suffers from the same difficulties as the triode modulator with regards to the setting of the quiescent bias level and sensitivity. Again, it requires a limiter stage.

To alleviate some of these shortcomings, the circuit of Figure 8 was proposed. Here, the comparator and modulator are in separate stages. The accuracy and sensitivity of the modulator were improved by a factor equal to the gain of the comparator stage. Depending on the particular type of pentode used, and the bias conditions, the modulator may or may not tend towards excessive or insufficient pulse generation.

All of the above systems produced single-polarity output pulses. Armstrong, in his thesis (2), designed and constructed a uni-polar system demonstrating the feasibility of delta modulation. Further work on uni-polar systems was also performed at the University of Texas in 1956 (34), and at the University of British Columbia in 1959 (6).

To produce a bi-polar output pulse train, the complexity of a delta modulation system is increased. Both of the aforementioned theses also described bi-polar systems.

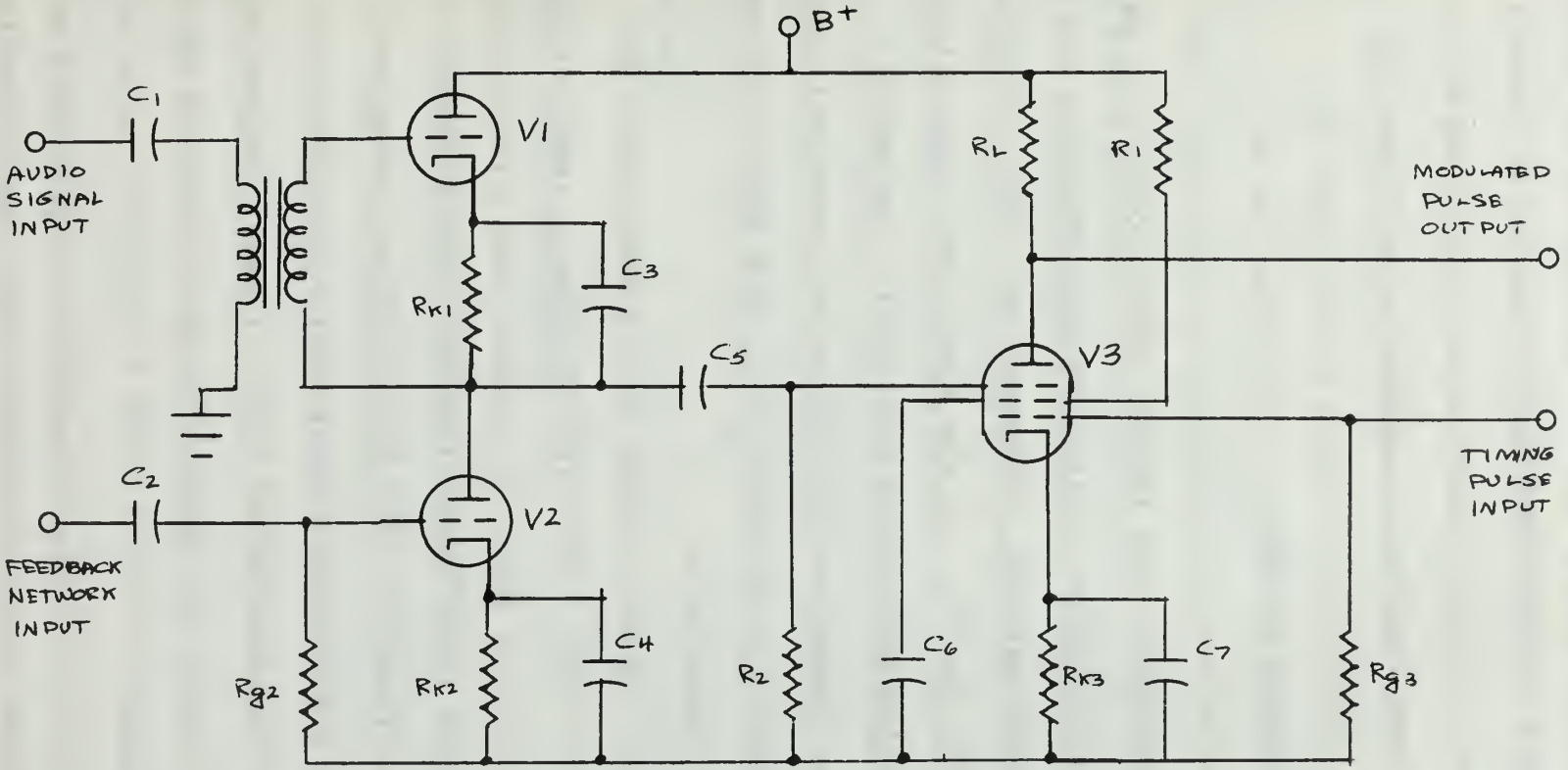


Figure 8: Single-ended Push-Pull Comparator and Pentode Modulator

Uni-polar systems have the advantage only if the pulse repetition rate is very constant. When it is variable (as when the signal is tape recorded and played back at uncertain speeds) both polarities should be provided (6).

B. TRANSISTORIZED SYSTEMS

Toward the end of the 1950's, delta modulation was used in limited applications. Circuits were designed and built for voice communications, telemetry and video transmissions (3-4, 6, 26-28, 34-35). At the same time, transistorized versions of delta modulation made their appearance.

Typical of these circuits was a voice-transmission system designed by F. W. Arter (3). The specifications for the system's design were:

1. Input---typical speech in the band width 300 - 3000 Hertz (Hz). The typical dynamic range of such signals is about 30 decibel (dB) with the average signal level some 12 dB below peak levels. The amplitudes of the signal peaks were about 1 V and the average signal amplitude about 0.25 V for representative input signals. Peak clipping to reduce the dynamic range to about 24 dB was allowed.
2. Transient response---capable of reproducing a 1000-Hz sinusoidal input signal with a maximum amplitude of 0.25 V.

3. Effects of quantization noise were not to produce an effective signal-to-noise ratio worse than 30 dB.

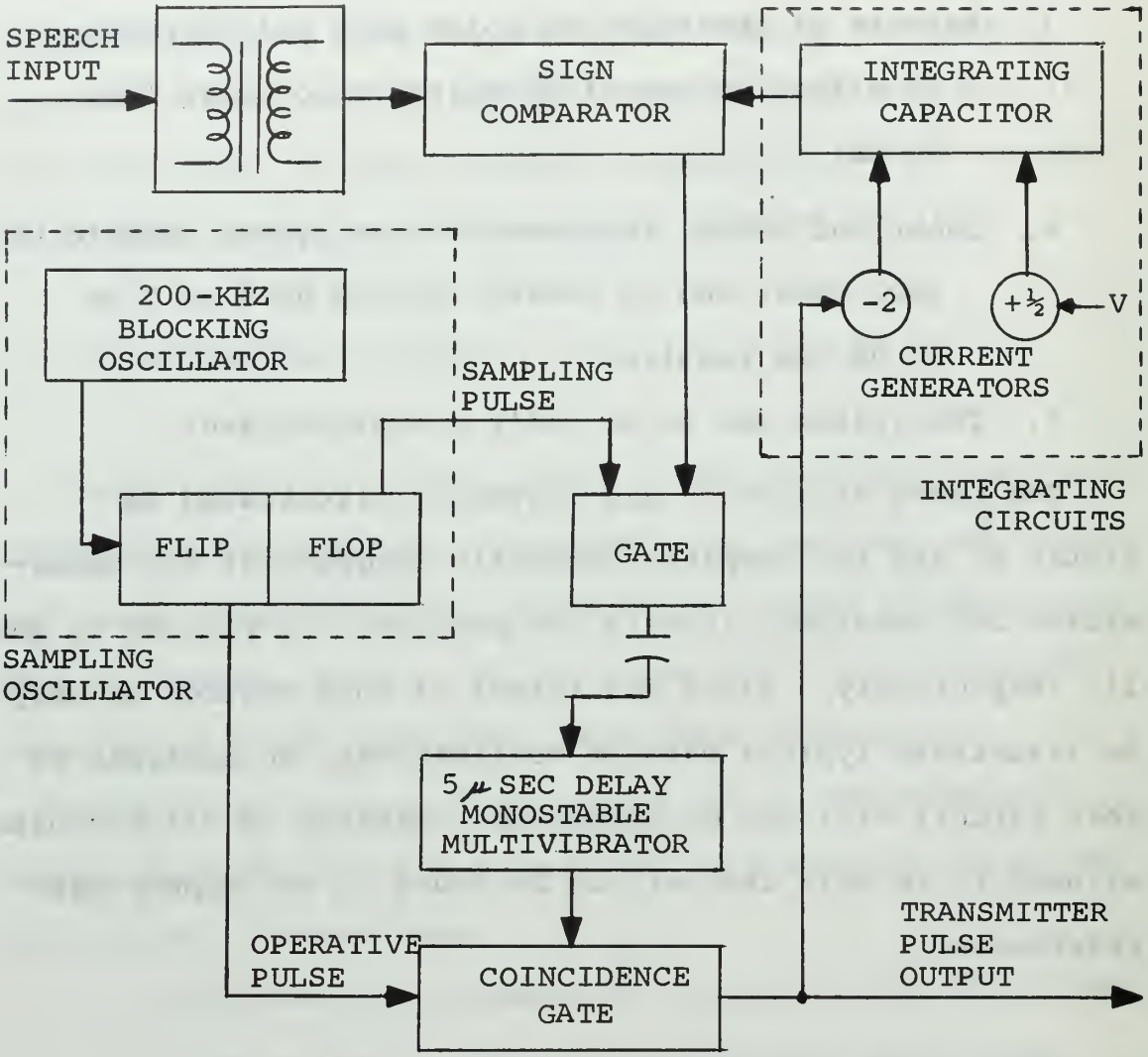
4. Input and output impedance of the system were to be 1200 ohms, and an overall system gain of 5 to 10 dB was required.

5. The system was to be fully transistorized.

The block diagram of the system is illustrated in Figure 9, and the complete schematic diagrams of the transmitter and receiver circuits are presented in Figures 10 and 11, respectively. Since the intent of this section is only to illustrate typical circuit realizations, an analysis of this circuit will not be presented. Details of all circuits alluded to in this chapter may be found in the appropriate references.

C. DELTA-SIGMA MODULATION

In comparing pulse modulation systems, pulse-code modulation has been considered the most efficient, although the circuitry used in modulation and demodulation is quite complicated and expensive. Delta modulation requires wider bandwidth than does PCM, but the circuitry is much simpler. An additional drawback of delta modulation is that transmission disturbances result in an accumulative error in the demodulated signal. This drawback has confined the use of



(a) Transmitter

(b) Receiver

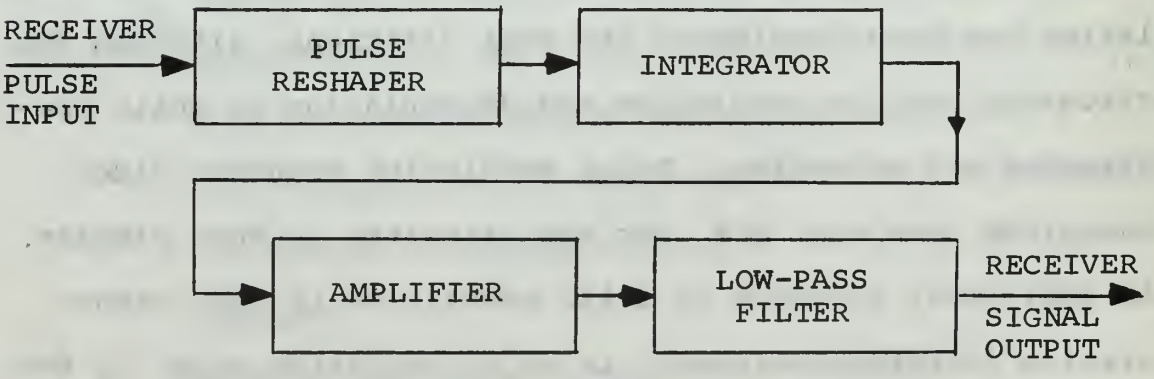


Figure 9: Block Diagram of the Voice-Transmission DM System

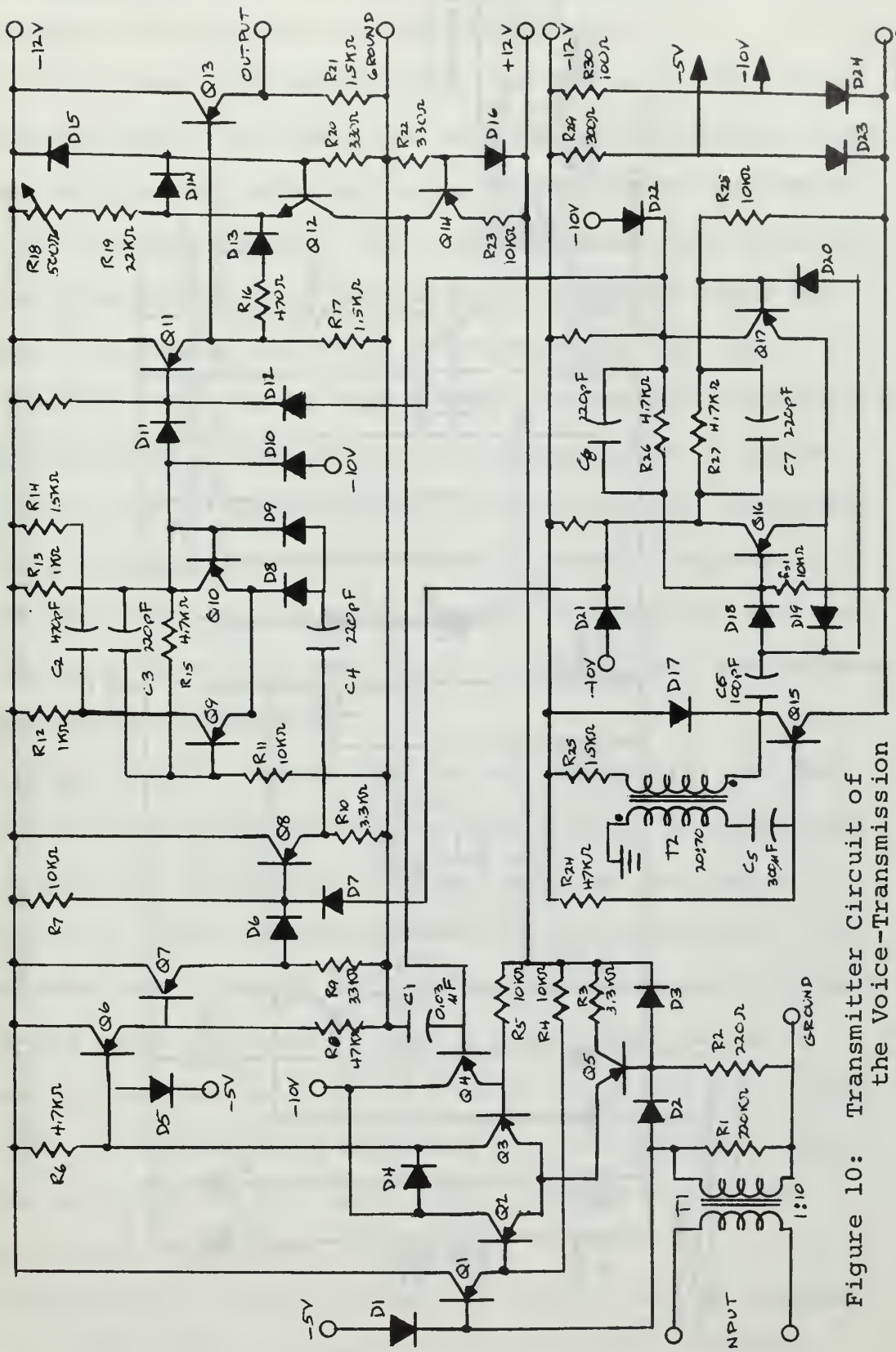


Figure 10: Transmitter Circuit of the Voice-Transmission DM System

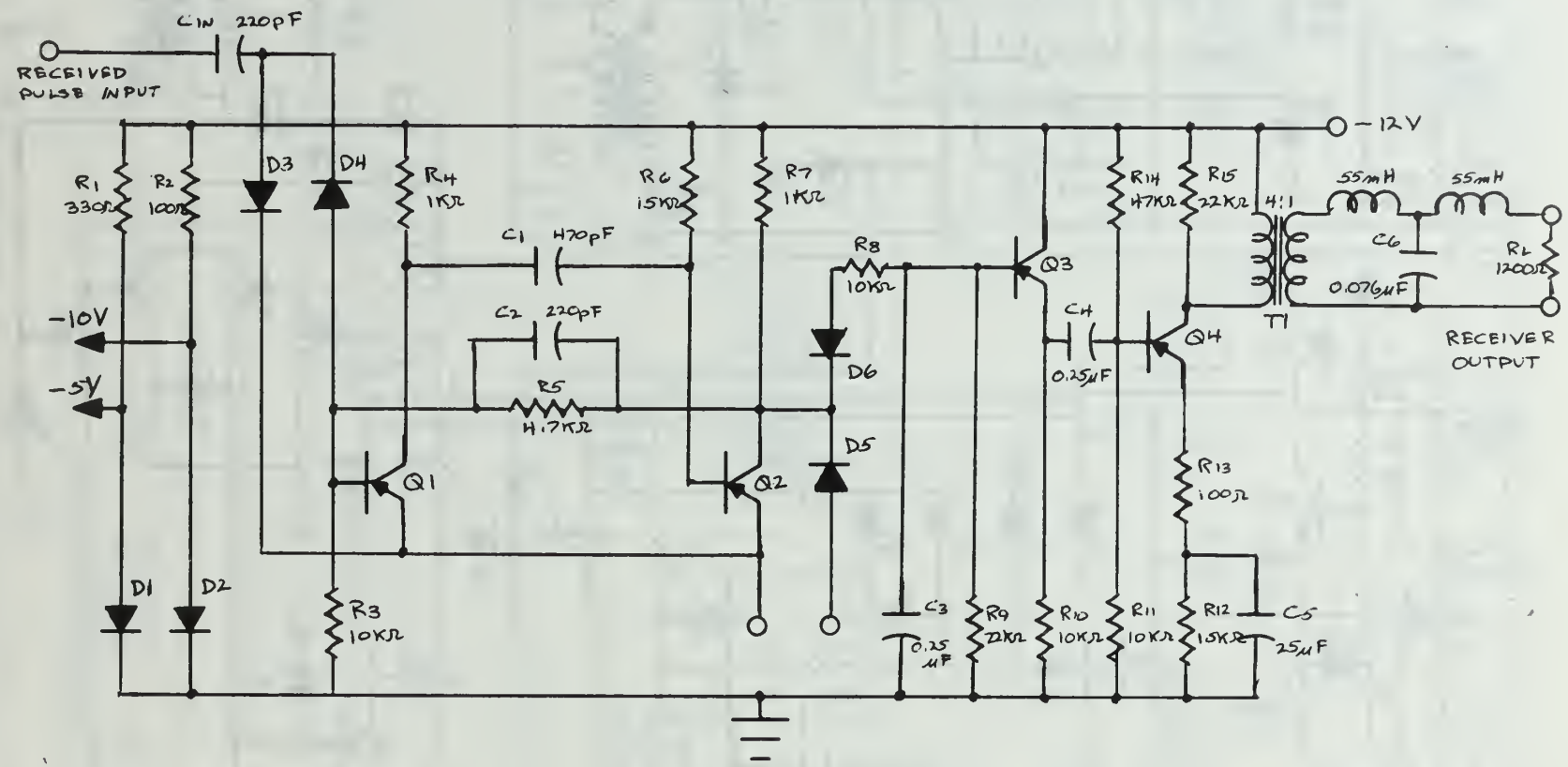


Figure 11: Receiver Circuit of the Voice-Transmission DM System

delta modulation to the transmission of signals which need not transmit the DC level of an input signal.

To eliminate this shortcoming, the input signal can be integrated before it enters the modulator to generate output pulses carrying the information corresponding to the amplitude of the input Signal. The realization of this principle is the Delta-Sigma (Δ -Σ) modulation system proposed by H. Inose, Y. Yasuda and their co-workers (21, 22, 23).

The block diagram of this system (Figure 12) consists of a feedback system composed of a pulse generator, a pulse modulator, and integrator and a low-pass filter. Referring to the conventional delta modulation system of Figure 1, it can be observed that the only changes of circuitry are the relocation of the integrator in the encoder, and the absence of the decoder integrator.

In the Δ -Σ system, the output pulses p(t) are fed back to the input and subtracted from the input signal s(t). The difference signal d(t) = s(t) - p(t) is integrated to produce e(t) which is applied to the pulse modulator. The pulse modulator compares e(t) with a predetermined reference level and opens the gate to pass a pulse from the pulse generator when the polarity of e(t) is positive, and closes the gate to inhibit the pulse when e(t) is negative. Hence, if the amplitude of the input signal becomes large, the output pulses occur more frequently.

Demodulation in the receiver is carried out by shaping the received pulses and passing them through a low-pass

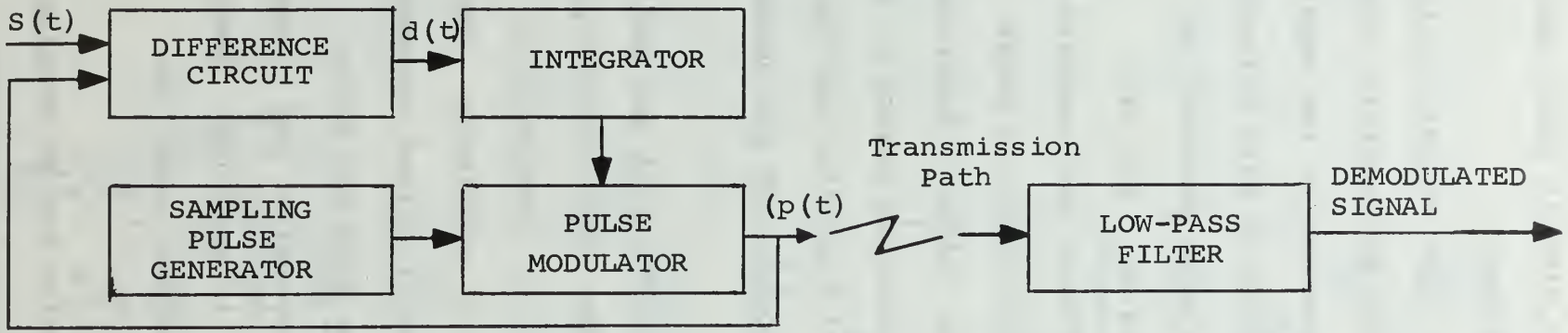


Figure 12: Block Diagram of Δ-Σ Modulation

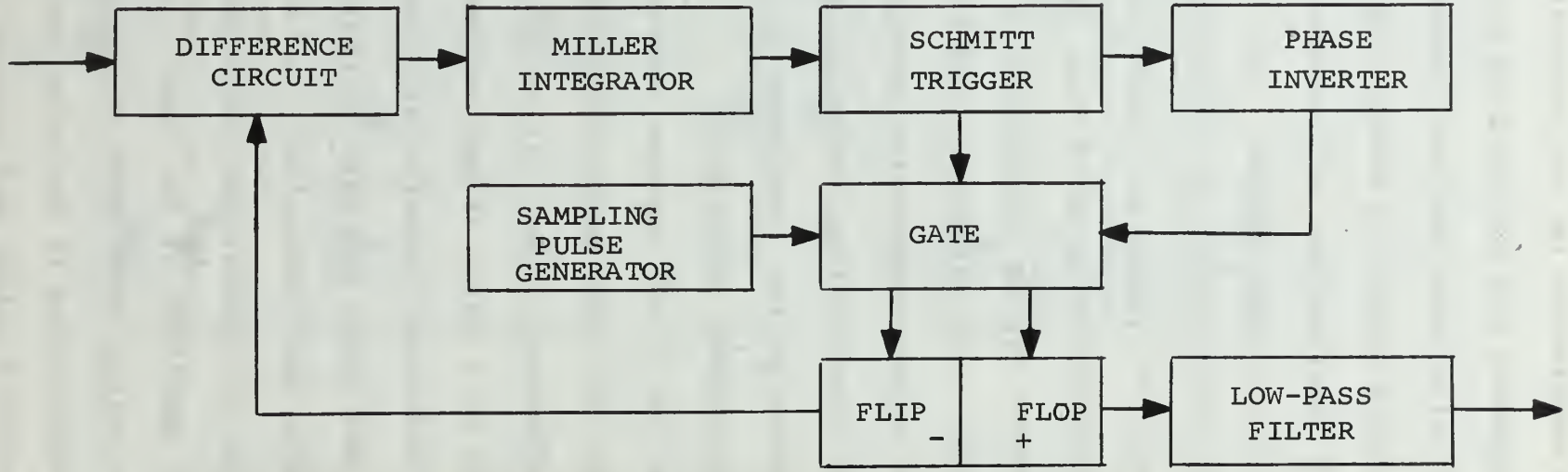


Figure 13: Block Diagram of the Δ - Σ Telemetry System

filter. No integration procedure is involved, therefore no accumulative error due to transmission disturbances results in the demodulated signal.

The authors have demonstrated the feasibility of Δ-Σ modulation for telemetry and video applications. The block diagram of their telemetry system is illustrated in Figure 13. This system was designed for an input signal frequency range of dc to 50 Hz with the repetition frequency chosen as 1 kHz. Built entirely with semiconductor components, the system was found to have a better performance stability compared to conventional delta modulation, although it requires essentially the same bandwidth and complexity of circuitry.

D. OTHER MODIFICATIONS

There have been several modifications of conventional DM proposed. The first, presented in 1953, encompassed the same amplitude quantization as DM, but was not quantized in time (25). Irving, in his thesis (24), found this synthesis method of encoding to have several advantages, but the method has not been incorporated in a system application.

In conventional DM, each pulse changed the approximating signal by one level only. Winkler, in a method called High-Information Delta Modulation (HIDM), has the number of level changes per pulse of the same polarity vary exponentially (36). The system can, therefore, respond quickly to

steep-slope signals thus reducing slope-limiting effects to near zero. An obvious disadvantage is the probability of high overshoot, especially with zero-rise-time input signals. HIDM has been used to transmit visual information between facsimile transmitters and receivers with good quality (37).

Lastly, de Jager and Greefkes have proposed a continuous DM system where the size of the quantization unit is varied in proportion to the input signal (9). This permits the use of lower pulse frequencies. Applications of this method have not yet appeared in the literature.

V. DELTA MODULATION WITH INTEGRATED CIRCUITS

Integrated circuits, by definition, consist of two or more inseparable elements, mounted on or within a common substrate, and connected together to form a single electrical network. With the aid of photographic reproduction, a discrete-component circuit requiring a large area can be replaced by a single integrated circuit (IC) approximately 50 mils square.

Each IC produced has the capability to perform specific tasks such as amplification, counting and logic implementation, to mention a few. With the addition of minor external modifications, their capability to perform a wide variety of functions is vastly increased.

To extend the evolution of delta modulation, a circuit incorporating IC's has been designed and constructed. A total of only five IC's were required to form a complete DM encoding system. The description of the four different types of IC's used and their internal circuitry can be found in the Appendix. The remainder of this chapter describes the functional sections of the system which have incorporated IC's.

A. INTEGRATED-CIRCUIT DELTA-MODULATION (ICDM) SYSTEM REQUIREMENTS

1. Clock (Pulse Generator)---to operate at 50 kHz; duty cycle of 0.1 to produce a 2.0-μsec positive pulse.

2. Comparator (Difference Circuit)---to compare input signal of one kHz with the system approximation signal; to generate a logical "ONE" or "ZERO" for input to the pulse modulator.

3. Pulse Modulator---to generate positive pulses at the clock frequency when a logical "ONE" is received; to generate negative pulses at the clock frequency when a logical "ZERO" is received. The output pulse train (with positive and negative polarities) is to be available at a single point in the circuit for transmission.

4. Integrator---to perform single integration to generate a staircase-like approximation signal for feedback to the comparator.

5. General---the inputs will consist of one-kHz sinusoidal and triangular waveforms. The system is to demonstrate the limiting characteristics of DM (slope limiting, minimum amplitude) and to utilize the minimum number of IC and discrete components.

B. CLOCK

Two Fairchild TTμL 9601 integrated circuits were chosen to construct the system clock. This circuit, a Retriggerable Monostable Multivibrator, is capable of producing a 50-nsec to infinity pulse width with a zero to 100% duty cycle. The pulse width, as indicated in the Appendix, is determined solely by the external time components, R_x and C_x.

In order that the clock pulses be produced continuously and without external triggering, the two 9601's were connected in the astable configuration shown in Figure 14. The lower portion of the figure depicts the waveforms appearing at each of the four outputs. The desired clock output is obtained at pin A_6 of 9601 "A."

To illustrate a typical cycle, consider initially a positive transition at pins A_3 and A_4 of 9601 "A." This transition completes the triggering requirements: pins A_1 and A_2 = "ZERO"; pins A_3 and A_4 = "ONE." Pin A_8 rises to and remains in the "ONE" state; pin A_6 becomes "ZERO." Triggering requirements are not fulfilled at 9601 "B"; thus pin B_8 is "ZERO" and B_6 is "ONE." The clock outputs will remain in the above states for the length of time determined by R_x-C_x. A pulse width of 2.0 μsec requires: C_x = 200pF, R_x = 25.0 kΩ for this period.

Upon completion of the above timing period, pin A_8 will fall to the "ZERO" state and pin A_6 will rise to the "ONE" state. This latter transition, connected to pins B_3 and B_4, completes the necessary requirements to trigger 9601 "B." The circuit operation following is similar to that above except that now the timing components R_y and C_y determine the timing period. A duty cycle of 10% requires a timing period between pulses of 18 μsec. (Clock frequency = 50kHz.) Component values are C_y = 1800pF and R_4 = 30.5kΩ for this timing period.

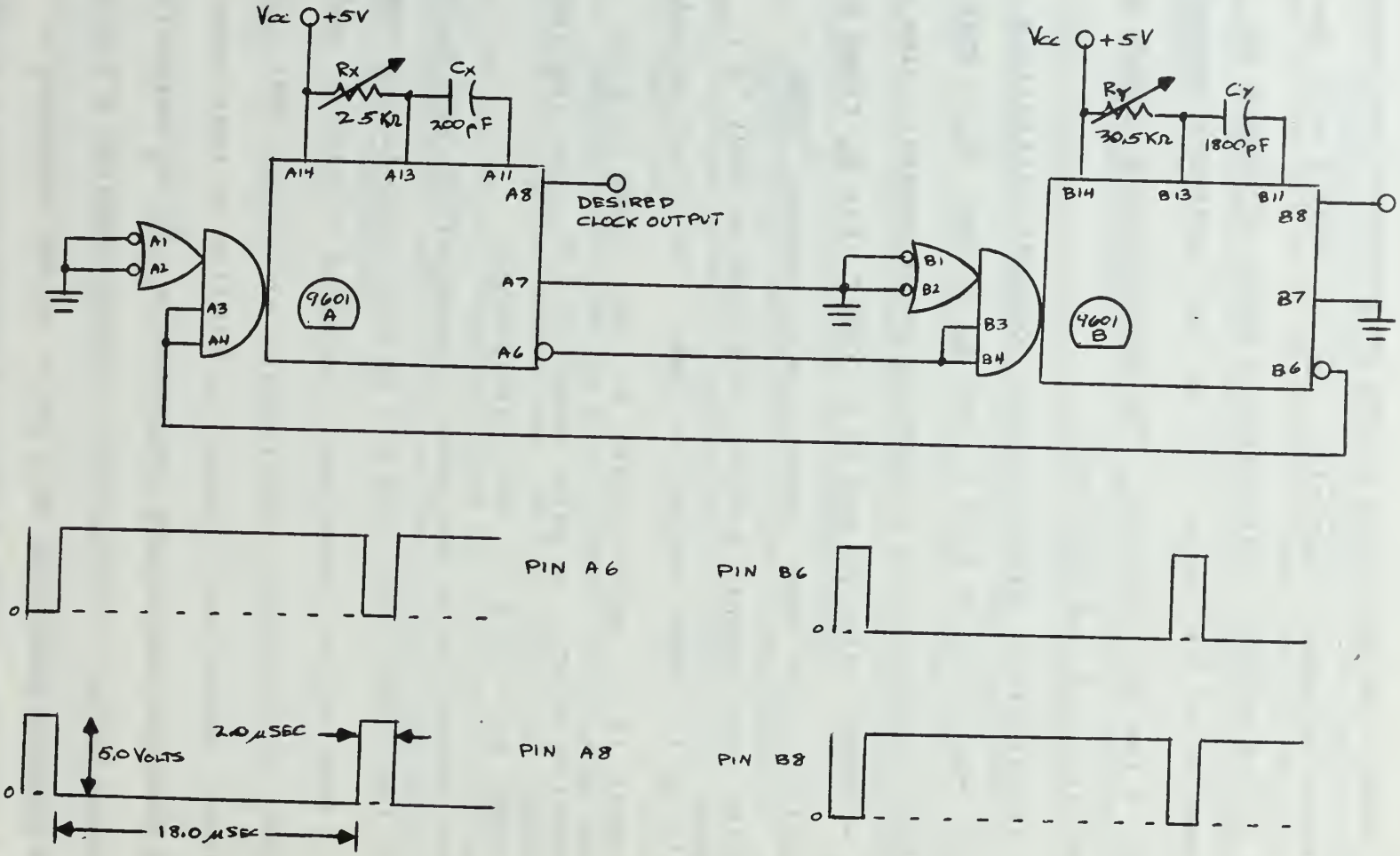


Figure 14: ICDM System---Clock and Available Waveforms

C. COMPARATOR

The μA710 High-Speed Differential Comparator fulfills the difference-circuit or comparator function without the need for external discrete components. A complete description of this IC's operation is presented in the Appendix. The pin configuration of the μA710 is depicted in Figure 15.

With bias voltages of $V^+ = 12$ v and $V^- = -6$v, the output voltage will be typically 3.2 volts when the input at pin two is greater than that at pin three. When pin three is greater in magnitude, the output voltage level is on the order of -0.5 volts. The maximum differential input voltage is limited to $\pm$ 5 volts, but as the integrator output signal will usually be quite close to realizing the input, the limit will only be of interest when slope limiting is present.

D. PULSE MODULATOR

With the clock and comparator inputs described above, the system is now ready to form the output pulses. Logic gates and clamping diodes have been used to perform this function. Four gates are required; all are available in one IC, the TTμL 9002. Each of the four independent gates implement the NAND logic function, producing a low output only when all inputs are high. Figure 16 depicts the construction of the pulse modulator. D1 and D2 are IN277

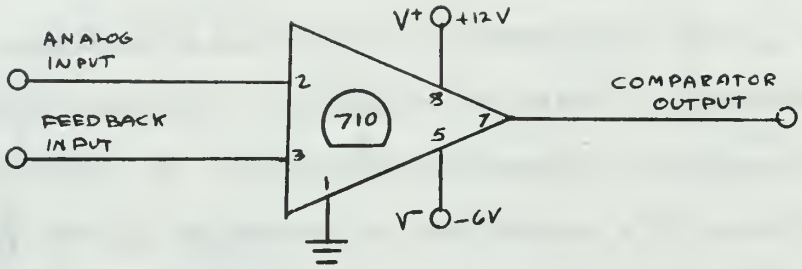


Figure 15: ICDM System---Comparator

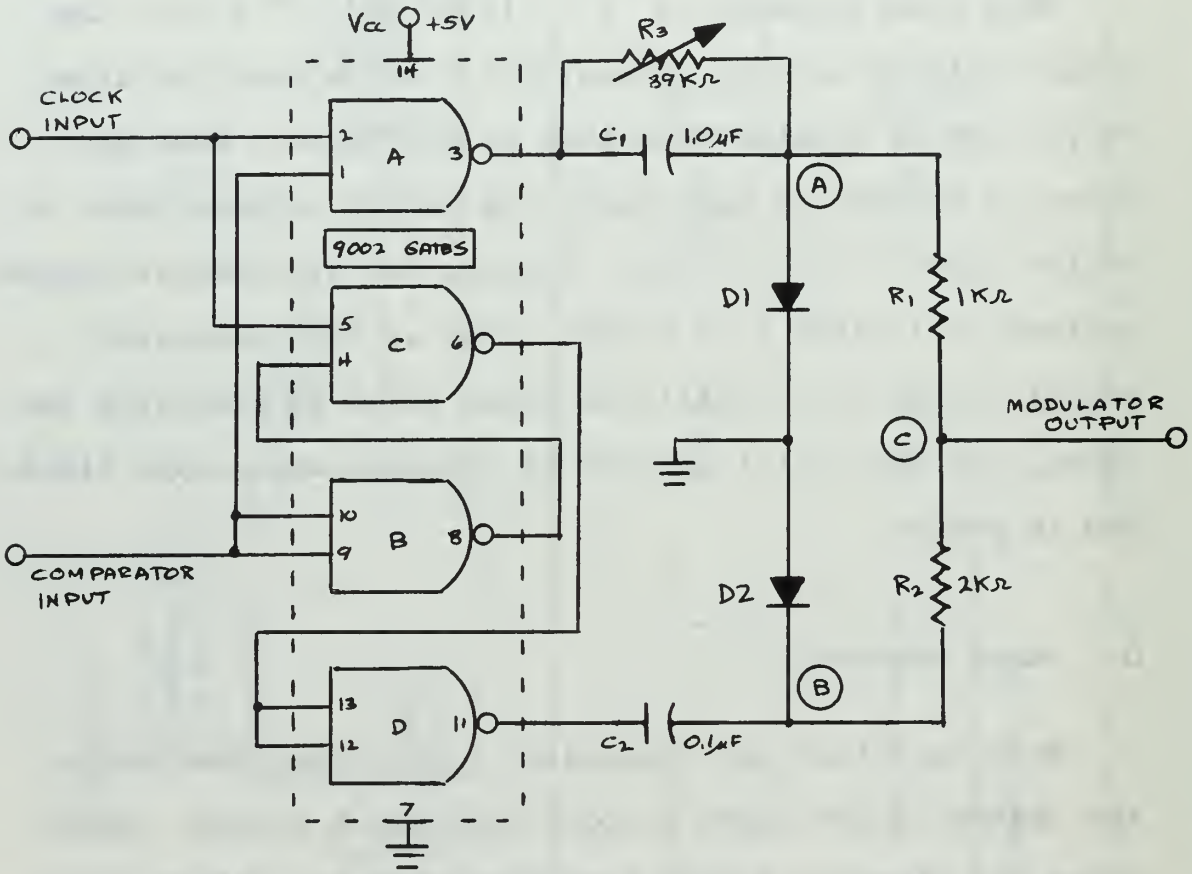


Figure 16: ICDM System---Pulse Modulator

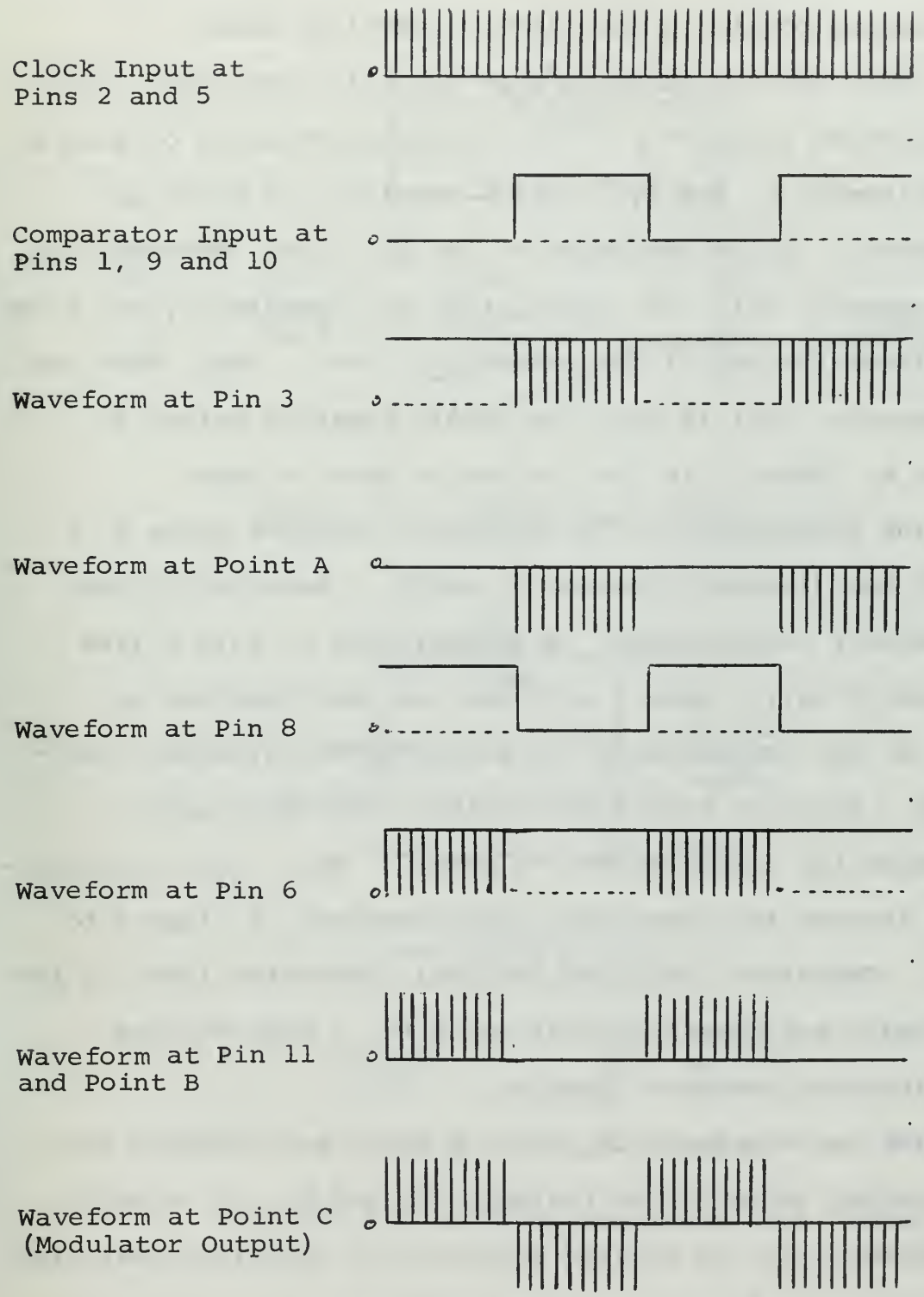


Figure 17: Waveforms in the ICDM System Pulse Modulator

germanium diodes. Figure 17 illustrates expected waveforms at various points in the circuit described below.

There are two paths through the pulse modulator, both terminating at point C. The first path consists of gate A and elements C_1 and R_1. Gate A receives the clock and comparator inputs and produces, at pin three, the waveform of Figure 17 (c). The combination of capacitor C_1 and diode D1 clamps the top of the waveform to zero. Thus, when the comparator level is high, we obtain negative pulses at point A. When it is low, we have a zero voltage.

The second path in the modulator involves gates B, C and D and discrete elements C_2 and R_2. Reversal of the comparator output states is accomplished by gate B (see Figure 17 (e)). Gate C performs the same function as Gate A, but now produces the pulses on the alternate half-cycle. Positive pulses are desired, therefore Gate D reverses the output states of Gate C. The C_2-D2 configuration insures that the base of the waveform is clamped to zero. Therefore, when the original comparator level is low, we obtain positive pulses at point B. A zero voltage results when the level is high.

The two waveforms at points A and B are combined into one output (point C) by resistors R_1 and R_2. A variable resistance, R_3, is located across C_1 to facilitate matching of positive and negative pulse amplitudes.

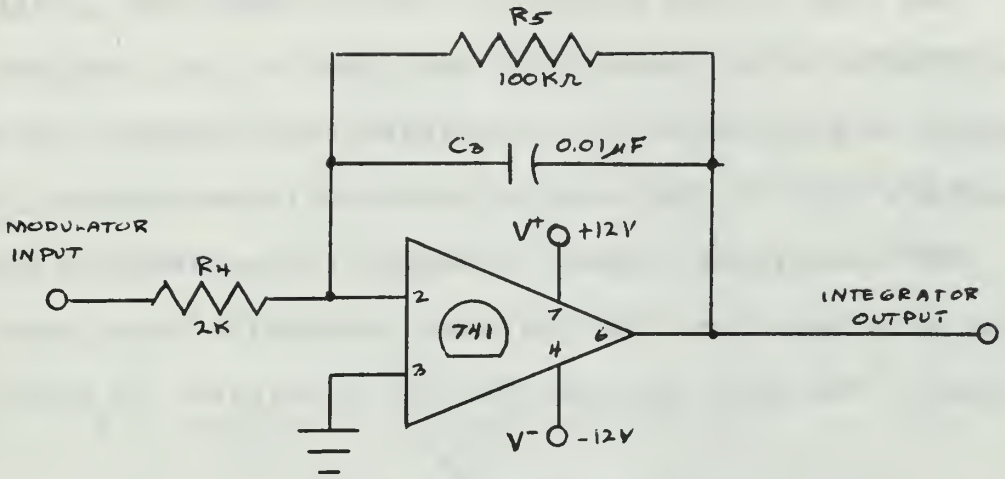


Figure 18: ICDM System---Integrator

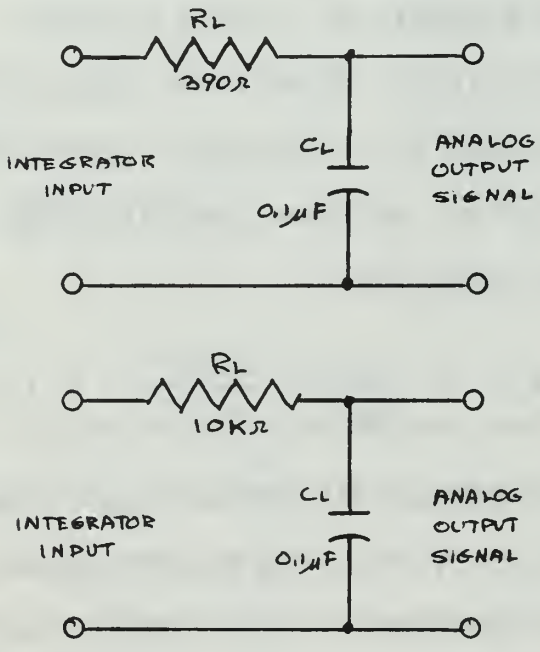


Figure 19: ICDM System---Low-Pass Filters

E. INTEGRATOR

The ICDM system integrator incorporates the μA741 High-Performance Operational Amplifier. In a complete system configuration, two integrators are needed, one in the feedback path of the encoder, and one in the decoder.

The integrator, shown in Figure 18, provides an output that is proportional to the time integral of the input signal. The gain function for the integrator is given by:

$$e_o = -\frac{1}{R_4 C_3} \int e_i \, dt$$

It is this relationship which determines the quantum step size of delta modulation in this system.

Consider a series of positive pulses with pulse width = 2 μsec and period T = 20 μsec. For the component values shown in Figure 18, we have the following output for each volt of input amplitude:

$$e_o = \frac{(1)T}{R_4 C_3} = \frac{2\text{x}10^{-6}}{2\text{x}10^{-5}} = 0.1 \text{ volts}$$

The charge associated with this rise in voltage is stored in the capacitor C_3. During the 18 μsec of the period in which a zero input exists, the charge leaks off slowly through R_5. The output voltage level will remain essentially constant; the small drop in voltage that does exist is governed by the time constant $R_5 C_3$ = 1000 μsec or 50 T. Thus, a series of positive pulses, when integrated, will

produce a rising staircase-like waveform. Similarly, a series of negative pulses will produce a descending staircase-like waveform.

The resistor, R_5, is included to provide direct-current (DC) stabilization for the integrator. Its function is to limit the low-frequency gain of the amplifier and thus to minimize drift (18). The frequency above which the circuit will perform as an integrator is given by:

$$f = \frac{1}{2\pi R_5 C_3} = \frac{1}{2\pi \times 10^{-3}} = 159 \text{ Hz.}$$

The size of the resistors R_4 (small) and R_5 (large) follows from the above description. The capacitance C_3, if large, minimizes the waveform decay, but also reduces step size. If a larger step size is desired with a small C_3, then the decay effects will be greater. Therefore, an arbitrary compromise value of 0.01 μF was chosen.

F. LOW-PASS FILTERS

In a complete DM system with both encoder and decoder, the integrators of each are designed to be identical. In the present system, the decoder was not built. In order to simulate the decoder (integrator plus low-pass filter), the integrator output was also fed to two low-pass filters as shown in Figure 19. The characteristics of the two filters are shown in Table I.

Table I

Theoretical Low-pass Filter (LPF) Characteristics
(for one kHz input sinusoid)

	Upper 3dB Frequency, f_2	Steady-state Gain, $\|A\|$	Phase Lead θ, degrees
LPF #1 R_L = 390 C_L = 0.1 μF	4.08 kHz	0.97	-13.8
LPF #2 R_L = 10 K C_L = 0.1 μF	159 Hz	0.16	-80.9

G. SYSTEM DIAGRAM

Figure 20 illustrates the ICDM system as formed by the elements described above. The system has incorporated the identical functional blocks as the encoder depicted in Figure 1. The following two chapters describe and discuss the results obtained with this system.

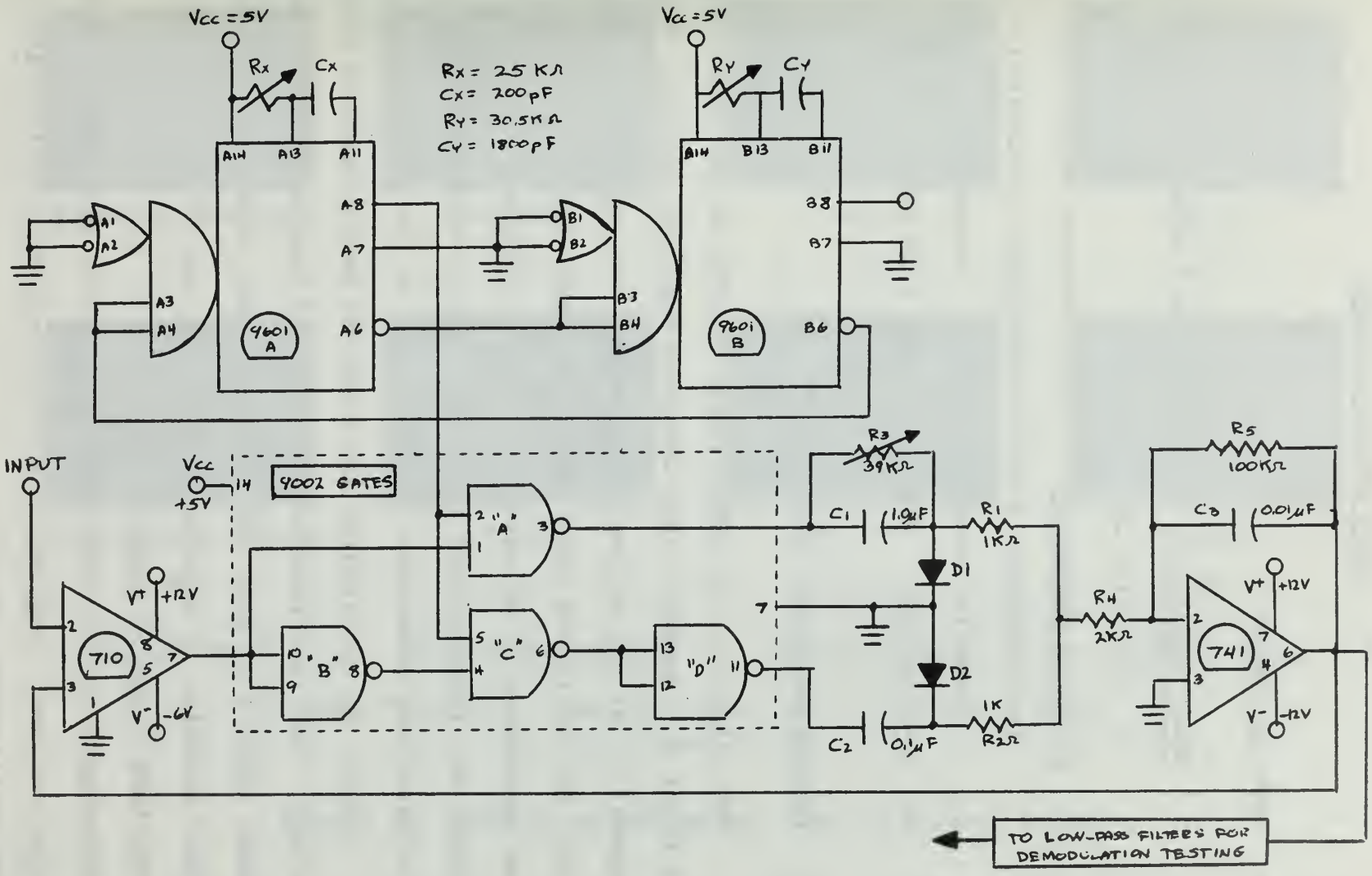


Figure 20: Integrated-Circuit Delta-Modulation System Diagram

VI. ICDM SYSTEM RESULTS

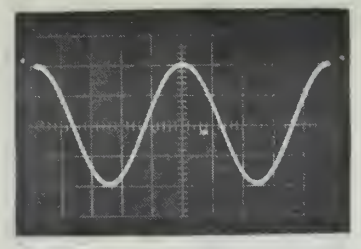
A. TEST EQUIPMENT

1. Power Supplies: Hewlett-Packard Model 721A. Range 0 - 30 volts DC.
2. Function Generator: Hewlett-Packard Model 202A. Low-frequency function generator; sinusoidal/triangular/square functions. Range 0.01 - 1200 Hz.
3. Oscilloscope: Tektronix Type 515A (single trace).

B. INTEGRATOR OUTPUT WAVEFORMS

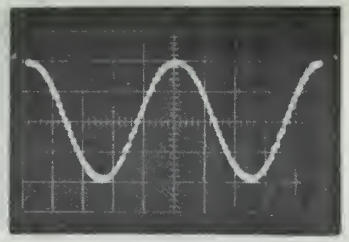
The output of the ICDM system encoder is the pulse train at Point C. However, this waveform does not indicate the capability of the system to reproduce the input after decoding. To facilitate this comparison, the "decoded" output was considered to be available at the integrator. This output was then applied to each of the low-pass filters; the resulting waveforms are described in the next section.

Figure 21 illustrates the expected performance of the system. The integrator was capable of producing almost an exact replica of both the sinusoidal and triangular one-volt input signals. A similar performance was obtained for an amplitude range of approximately 0.25 to 1.5 volts. (All photographs in this section have the time axis running from right to left. This was due to the mounting configuration of the oscilloscope camera.)



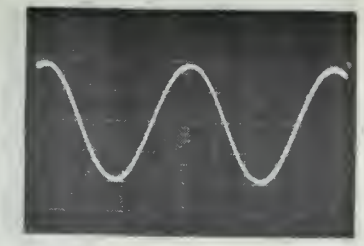
Sinusoid:;V=1.00

(a)



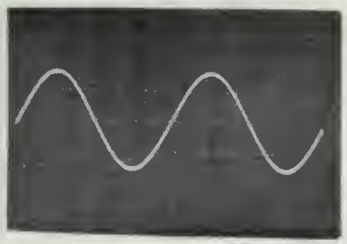
V=1.00

(b)



V=0.98

(c)

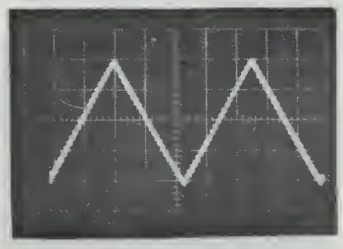


V=0.16

(d)

Triangular: V=1.00

(e)

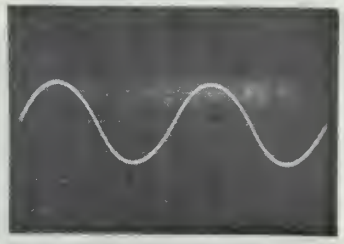


V=1.00

(f)

V=0.95

(g)



V=0.14

(h)

System Input | Integrator Output | LPF #1 Output | LPF #2 Output

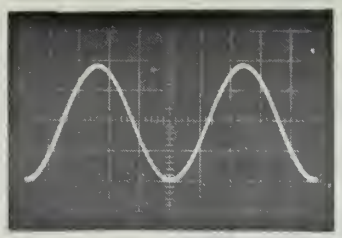
Scales: Hor - 0.2 msec/cm; Vert - 0.5 V/cm (a-c, e-g), 0.1 V/cm (d, h)

Figure 21: Output Waveforms for One-Volt Input Signals

As the amplitude of the input signal is increased, the effects of slope limiting become evident. This is illustrated by the integrator waveforms of Figures 22 and 23. The integrator cannot reproduce the input waveforms in all four cases illustrated. The apparent reproduction of the triangular inputs occurs only because a slope-limited signal resembles a triangular wave.

In the previous chapter, it was stated that after the integrator output had risen or fallen by the quantum step size, the waveform would decay only slightly. The percentage of decay (about 2%) is constant in all situations. However, the magnitude of the change is larger for increasing amplitude. This is also illustrated in the integrator waveforms of Figures 22 and 23, by the slight curvature of the staircase waveforms.

For all slope-limited signals the step size was measured as 0.16 volts, with the pulses at Point C having an amplitude of 1.8 volts. As the amplitude of the system input decreased, and with the feedback signal capable of matching this input, the step size was found to decrease. Figure 24 illustrates the response to a very small input signal. With the reduced step size, the integrator output does produce an approximation of the input, instead of the expected waveform of alternate positive and negative steps. Actually, it appears that a full step of approximately 0.16 volts occurs, but immediately drops back to a fraction of this value. This

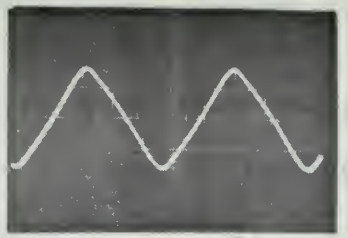


Sinusoid: V=2.00

(a)

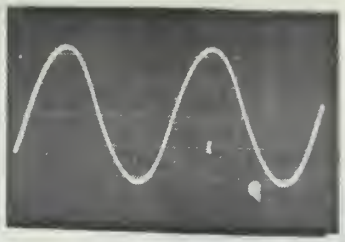
V=1.75

(b)



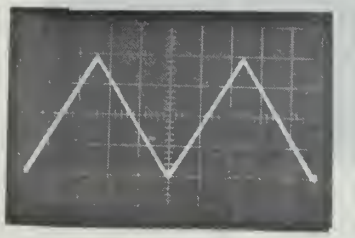
V=1.70

(c)



V=0.23

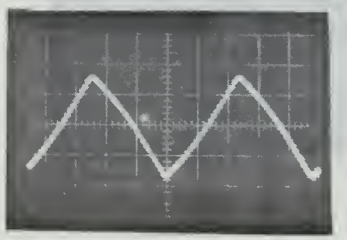
(d)



Triangular: V=2.00

(e)

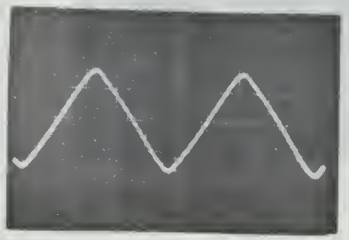
System Input



V=1.70

(f)

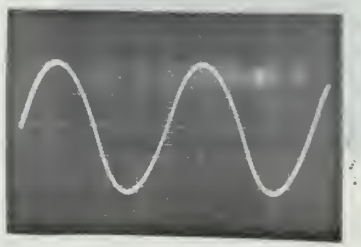
Integrator Output



V=1.70

(g)

LPF #1 Output



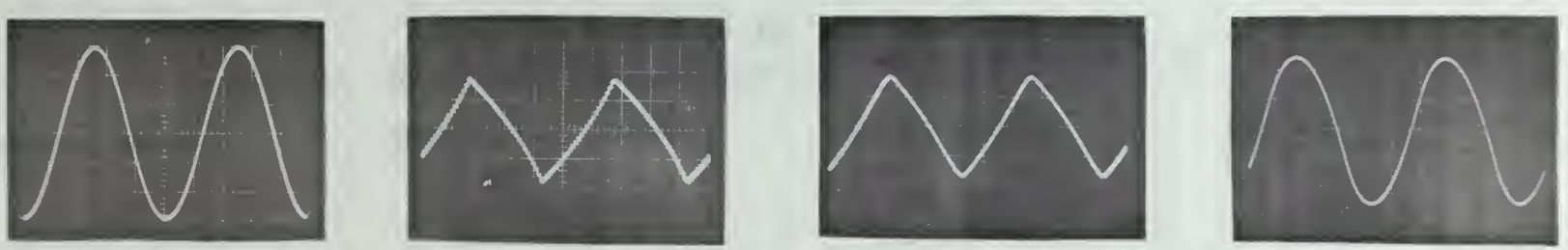
V=0.22

(h)

LPF #2 Output

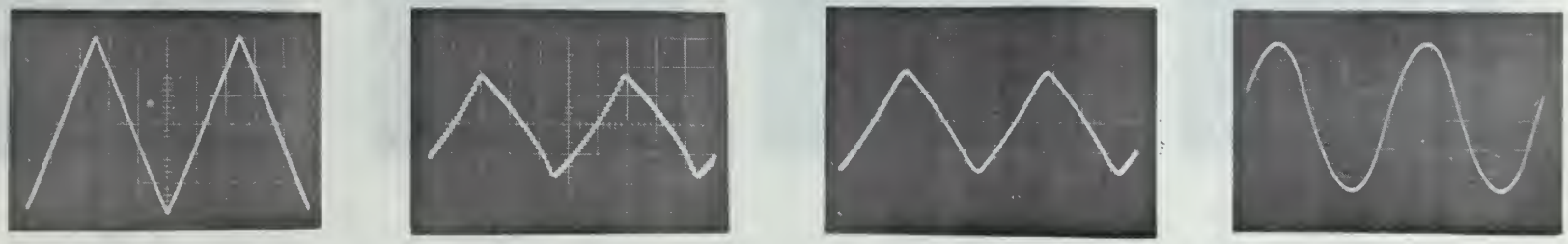
Scales: Hor - 0.2 msec/cm; Vert - 1.0 V/cm (a-c, e-g)
0.1 V/cm (d, h)

Figure 22: Output Waveforms for Two-Volt Input Signals



Sinusoid: V=3.00 V=1.80 V=1.78 V=0.25

(a) (b) (c) (d)



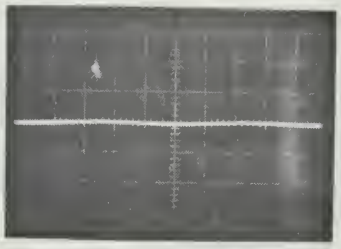
Triangular: V=3.00 V=1.80 V=1.78 V=0.25

(a) (f) (g) (h)

System Input Integrator Output LPF #1 Output LPF #2 Output

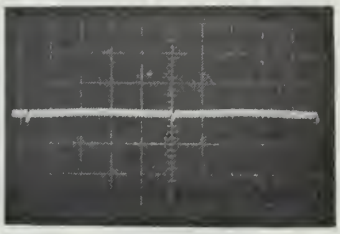
Scales: Hor - 0.2 msec/cm; Vert - 1.0 V/cm (a-c, e-g), 0.1 V/cm (d, h)

Figure 23: Output Waveforms for Three-Volt Input Signals



Sinusoid Input

V=0.01

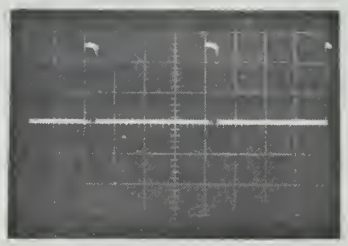


Integrator Output

V=0.02

Scales: Hor - 0.2 msec/cm; Vert - 0.1 V/cm

Figure 24: Output Waveform for 0.01-Volt Sinusoidal Input



Clock Output

V=5.2

Scales: Hor - 5 μsec/cm
Vert - 2 V/cm

Comparator Output

V=3.2

Scales: Hor - 0.2 msec/cm
Vert - 2 V/cm

Figure 25: Clock and Comparator Waveforms

is faintly visible on the oscilloscope, but is not evident in the photographs. (See the discussion in the next chapter.)

C. LOW-PASS FILTER WAVEFORMS

The two low-pass filters previously described were designed for the purpose of illustrating the effects of two different upper 3-dB frequencies (f_2). LPF #1, with f_2 = 4.08 kHz, was capable of passing sufficient harmonic content to reproduce any input applied to it. This is illustrated by the photographs (c) and (g) of Figures 21-23. A filter of approximately this size would be required for any waveform with harmonic content.

LPF #2, with f_2 = 159 Hz, was only capable of passing an attenuated fundamental frequency of the applied input signals. Photographs (d) and (h) of the same figures indicate this effect. The observed characteristics of both filters are listed below in Table II. (Note: All values are approximate.)

The component values for each of the above filters were chosen arbitrarily. In an operating system, however, the filter design would be subjected to a more detailed analysis procedure.

Table II

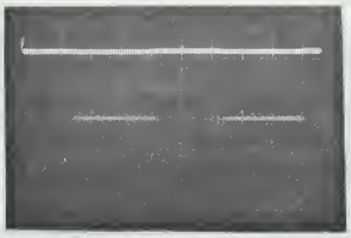
Observed Low-pass Filter (LPF) Characteristics
(for 1-kHz input sinusoid)

	Steady-state Gain, $\|A\|$	Phase Lead θ, degrees
LPF #1 R_L = 390 Ω C_L = 0.1 μF f_2 = 4.08 kHz	0.96	-15
LPF #2 R_L = 10 KΩ C_L = 0.1 μF f_2 = 159 Hz	0.16	-86

D. SYSTEM INTERNAL WAVEFORMS

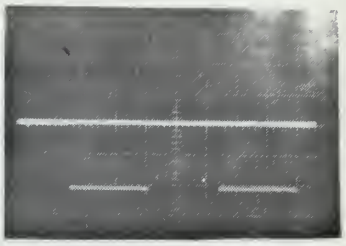
Figures 25 and 26 depict the waveforms present at various indicated points in the circuit. All photographs were taken for a two-volt sinusoidal input signal in order to obtain distinct waveforms (see Figures 14 and 17 for comparison with theoretical waveforms).

As input signal amplitude was decreased, the waveform of the comparator became difficult to interpret. The two output levels were still present, but a distinct pattern was not visible. All efforts to synchronize the oscilloscope with the waveform failed. The waveform patterns in the modulator were also affected. The output waveform at Point C appeared to have both positive and negative pulses



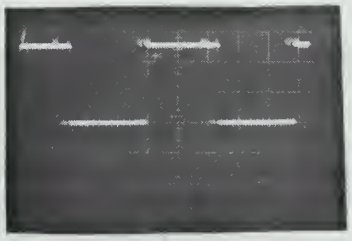
Pin 3: V=4.5

(a)



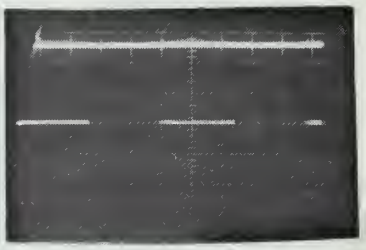
Point A: V=4.2

(b)



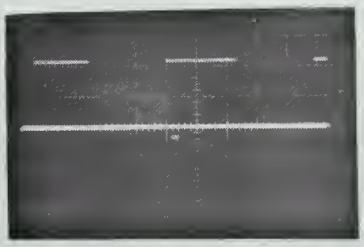
Pin 8: V=5.2

(c)



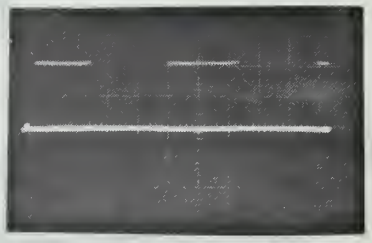
Pin 6: V=5.2

(d)



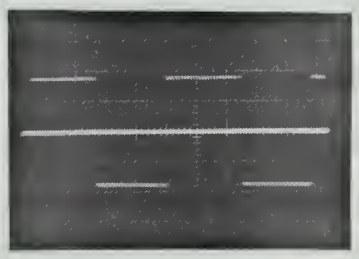
Pin 11: V=4.4

(e)



Point B: V=4.2

(f)



Point C: V=1.8

(g)

Scales: Hor - 0.2 msec/cm; Vert - 2 V/cm (a-f), 1 V/cm (g)

Figure 26: Pulse Modulator Waveforms

occurring at the same time. No photographs were possible due to the instability of oscilloscope presentation.

E. SYSTEM GROUND PLANE

Extraneous signals from the laboratory ground, the circuit power supplies and the function generator were encountered in the system ground circuit during initial testing. These signals were virtually eliminated by the use of a wire-mesh ground plane.

VII. DISCUSSION OF RESULTS

A. GENERAL

The Integrated-Circuit Delta-Modulation System was capable, despite the instability problem discussed below, of producing Delta Modulation. The system, at present, is only rudimentary. Detailed evaluation of the circuit design, such as signal-to-noise ratios, voice or telemetry input testing, etc., must await system refinements.

Comparison with research performed by others is difficult for several reasons. Delta modulation incorporating IC's has not been attempted previously (or at least not reported in the literature), possibly due to its limited applications. Therefore, direct comparison of circuit capabilities is not feasible. Due to the limited scope of this thesis, only a photographic comparison can be made, at present, with earlier discrete-component systems. Lender and Kozuch (26), and Watson and Hudson (34) have presented photographs in their reports, with the former the most detailed. Comparison with other systems described earlier would, in most cases, require a more detailed system study.

B. SYSTEM STABILITY

Slight deviations of the system clock from the nominal 50-kHz frequency could have the effect of varying the

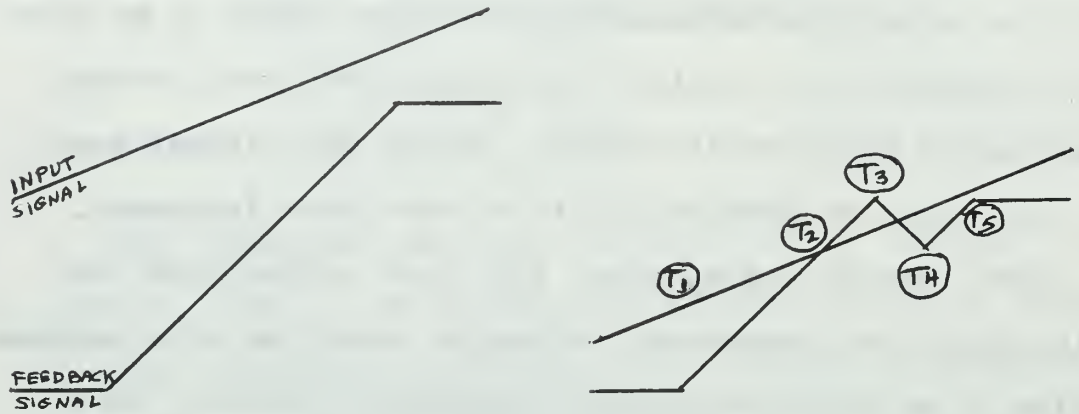
number of samples during a given cycle of input frequency. While not affecting the capability of the system to perform delta modulation, a constant (or repetitive) oscilloscope presentation would be difficult. During the circuit testing, there was no observed drift of the clock frequency.

Inose, Yasuda and Murakami (22) have stated that the variation of the comparator reference level can be a serious problem in an analog-to-digital conversion device. In a DM system, this variation (the feedback signal) is required. In the present system it appears that the observed system instability is probably caused by the comparison function.

The left half of Figure 27 illustrates the system waveforms under slope-limiting conditions. The input is always greater than the feedback signal from the integrator. The comparator output is always high, and the system produces a negative pulse 2-μsec wide at Points A and C. After integration, the approximation makes a quantum step in the positive direction. (The expanded time scale of Figure 28 illustrates that the step is actually a steep ramp).

Response times of the individual IC's are quite fast. A total system response would, at worst, be on the order of 0.5 μsec, or about one-fourth the pulse width (12, 14, 15).

In the right half of Figure 27, the two inputs are much closer at the beginning of the pulse cycle. At time instant T_1, the comparator output is high, opening Gate A to allow

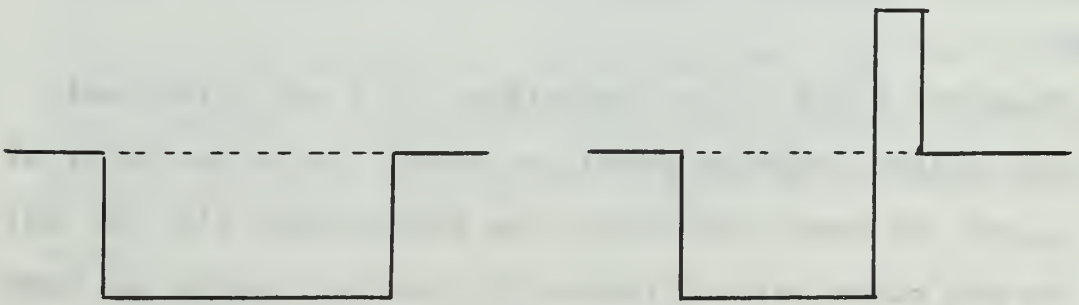


(a) Comparator Inputs

(b) Comparator Output

(c) Point A - Waveform

(d) Point B - Waveform



(e) Point C - Waveform

Figure 27: Waveforms Resulting from Normal and Unstable Comparator Level Sensing

a negative pulse to start forming at Point A. Gate B is closed at this instant of time. The integrator begins its positive ramp output.

At T_2, the feedback signal rises above the input signal. Once the comparator logic threshold level is exceeded, the comparator output state switches. This action closes Gate A and opens Gate B. As a result, the negative pulse being produced at Point A is cut off, and a positive pulse is started at Point B. The integrator input reverses, and now produces a negative ramp output. (Delay in the system does occur, but is not illustrated here).

The feedback signal again crosses the input signal and at T_4 the system is required to reverse states again. At T_5, the clock pulse is cut off, both gates are closed, and the integrator, with zero input, is now in its long exponential decay period. The net change or "step" of this waveform is approximately two-thirds of the change produced in slope-limiting.

It is felt that the above oscillatory motion of the comparator, occurring during the 2-μsec pulse interval, is the cause of the oscilloscope waveform instability. Delta modulation is occurring, but for each cycle of input, a slightly different output is produced. The oscilloscope, requiring a constant or repetitive input, is unable to reproduce a steady presentation.

It is evident from Figure 27, that, in order to eliminate the oscillations, the comparator must be made to remain in its initial state during production of an output pulse. It is possible that a more complex comparator can eliminate the instability. The μA710, with additional circuitry using the clock pulse to inhibit a change of output levels, may be sufficient. Fairchild also produces a μA711 Dual Comparator with four inputs and one output. Whether or not this IC would be needed is not known at present. It is suggested that future study of ICDM systems be concentrated on this problem.

VIII. CONCLUSION

In this thesis, it has been demonstrated that a delta modulation system incorporating integrated circuits is possible. The solution of the stability problem appears feasible, but requires additional study before implementation.

It is unnecessary, in this paper, to make recommendations for applications of delta modulation. The many references cited have probably exhausted this field. Instead, this thesis has attempted to demonstrate, by use of a rudimentary system, that many of these DM applications are now capable of utilizing integrated circuits in their design.

The literature on integrated circuits deals primarily with fabrication and usually has very little information to provide on actual applications. Those applications which are described, generally involve only one or two IC's at a time. In this paper, the design of a system utilizing four different (five total) IC's has been accomplished with the ICDM system.

APPENDIX A

DESCRIPTION OF INTEGRATED CIRCUITS

A. 9601 RETRIGGERABLE MONOSTABLE MULTIVIBRATOR; FAIRCHILD TRANSISTOR - TRANSISTOR MICROLOGIC INTEGRATED CIRCUIT (16, 17).

The TTμL 9601 is a DC level-sensitive retriggerable monostable multivibrator (one-shot) which provides an output pulse whose duration and accuracy is a function of the external timing components only. It has four inputs, two of which are active-level HIGH and two active-level LOW. Complementary outputs are provided.

The block diagram of the circuit is shown in Figure A-1. The trigger input gating is DC-coupled and independent of input transition times. Both true and complemented inputs are provided. The output transition of the input gating circuitry is converted to a pulse by the differentiator. As a consequence of this action, the input and output periods are independent.

The discharge circuit receives a short pulse from the differentiator and discharges the timing capacitor, C_x, to initiate a timing cycle. Since long delay periods require a large capacitance and long discharge time, the discharge circuit must continue to discharge the capacitor until the current drops to a fixed value. The discharge circuit is

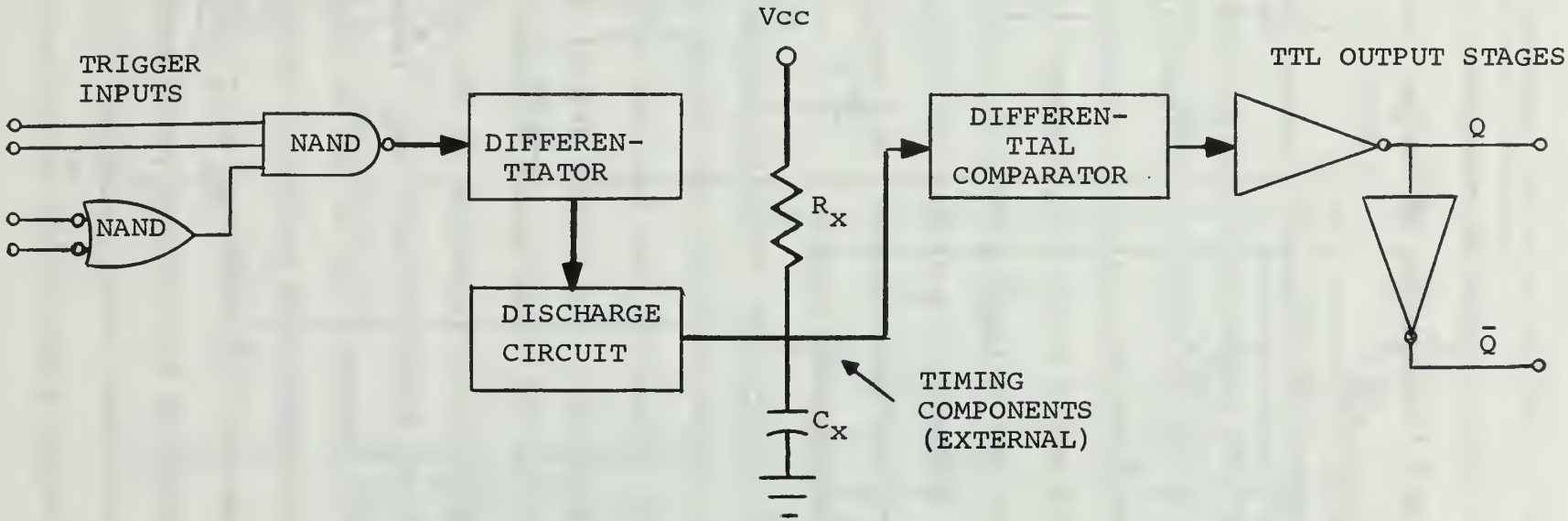


Figure A-1: Block Diagram of the TTμL 9601 Retriggerable Monostable Multivibrator

thus similar in action to a silicon-controlled rectifier. Whenever an input trigger is received, capacitor C_x first discharges and then begins to charge toward V_{CC} through the timing resistor R_x.

The differential comparator senses the voltage across C_x and holds the output high through TTL output stages while the voltage of C_x is below a differential threshold. The action is retriggerable since an input trigger will discharge C_x and begin a new delay cycle, independent of the output. When the voltage across C_x reaches a set fraction of V_{CC}, the comparator switches and drives the output through the TTL output stages. The output is also inverted to give a complemented output.

Figure A-2 shows the complete schematic diagram of the 9601. Input gating provides two inputs that will trigger on a positive transition and two that will trigger on a negative transition. The inputs are of the typical TTμL type; triggering will take place whenever Q4 is driven ON.

Due to inherent limitations of TTL processes, special treatment of the differentiator and discharge circuits was required. One proposal was to use an RC differentiator and a PNPN silicon controlled rectifier (SCR). There are two drawbacks however: 1) since the R_1C_1 combination is dominant in determining the minimum pulse width of the device, and since integrated circuit component tolerances are loose, the minimum output pulse width would vary with each device,

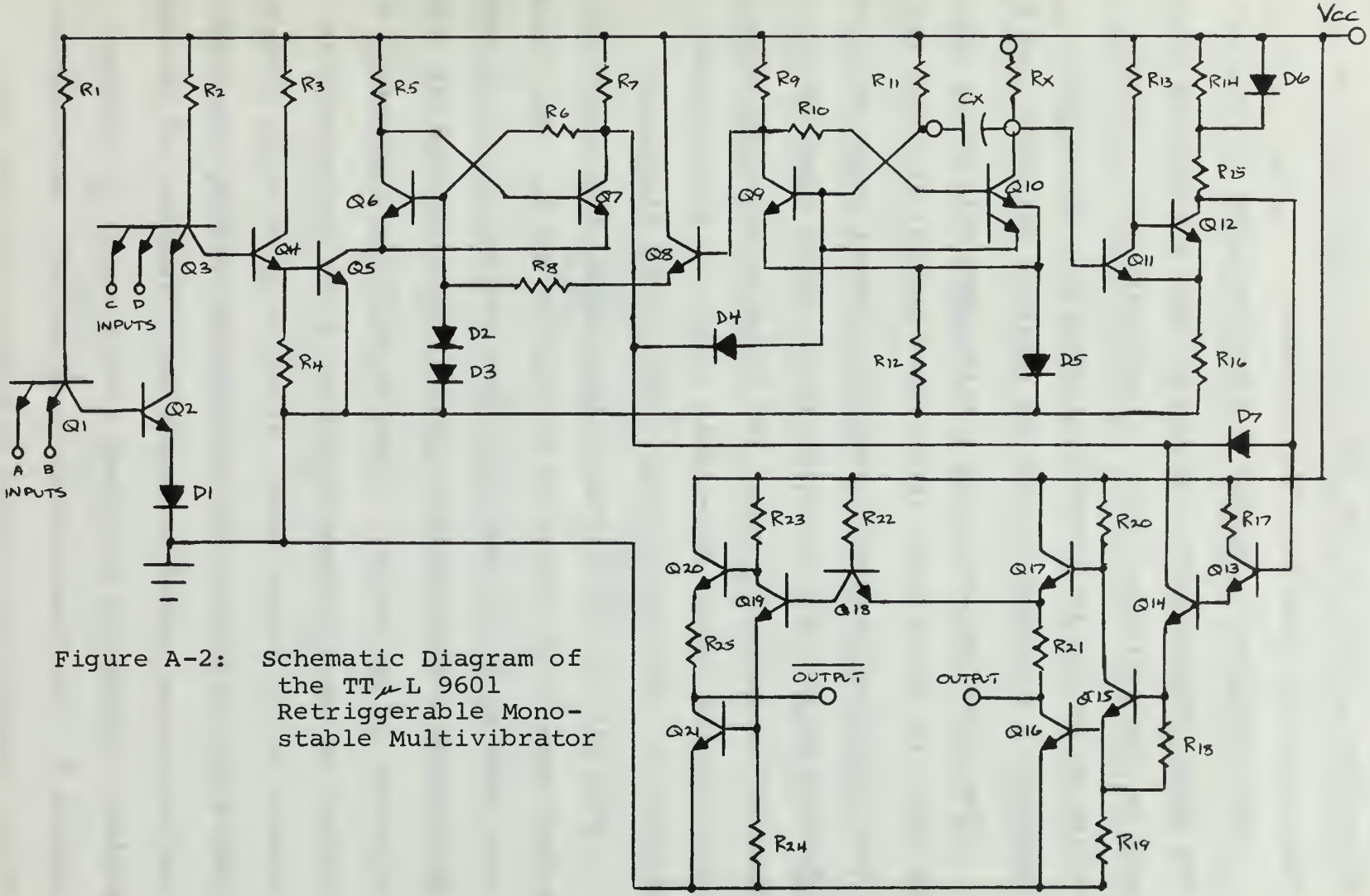


Figure A-2: Schematic Diagram of the TTμL 9601 Retriggerable Monostable Multivibrator

2) the PNP portion of the SCR (Q2) is impractical to fabricate with standard TTL processes.

The circuitry in Figure A-2 was designed to eliminate the above shortcomings. Q6 and Q7 form a flip-flop which acts as the differentiator. A monostable multivibrator, acting as an SCR is formed by transistors Q9 and Q10. Feedback is provided through Q8 (emitter follower) and R_8.

The flip-flop is in its stable state with Q6 ON and Q7 OFF. If the trigger (from input gating) is high, the diode D4 is back-biased. When the trigger drops to ground, Q7 turns ON and sets the flip-flop. Diode clamp D2-D3 ensures the correct state. The SCR-equivalent monostable then switches to its non-stable state, as Q9 turns OFF through D3, and remains there until C_x is discharged.

With Q10 ON, the differentiator-equivalent flip-flop resets when Q6 is driven ON through Q8 and R_8. The resistance ratio R_8/R_6 is such that Q10 is in saturation before Q6 turns ON. The discharge path of C_x is through R_{11}, the collector of Q10 and D5. After C_x has lost sufficient charge, D4 again becomes back-biased and the monostable returns to its stable state, allowing C_x to begin charging toward V_{cc}. Since R_{11} is much smaller than R_x, the initial discharge period is only a small fraction of the total period. During the principal timing cycle, C_x charges through R_x, the base emitter of Q9 and D5. Retriggering occurs whenever the trigger is brought high and then

returned to ground. If C_x is not present, the monostable returns to the stable state as soon as the differentiator flip-flop resets.

The extra emitter of Q10 is designed to provide a fast discharge path when the capacitor (C_x) voltage exceeds a certain value. This maintains the initial discharge period nearly constant. The end result of the design provides a differentiator which delivers a trigger pulse of optimum length and an SCR equivalent discharge circuit which can handle all values of C_x.

The differential comparator is an emitter-coupled Schmidt trigger formed by Q11, Q12, R_{13}, R_{15} and R_{16}. The trigger level V_T is given by the expression (17):

$$V_T = \frac{(V_{cc} - V_d)\, R_4}{\frac{R_1 R_3}{R_1+R_3} + R_4} + V_{BE(Q11)}$$

where V_d is the voltage across Q12 and D6 in parallel. Since Q12 is saturated, the V_{CE} of Q12 has been neglected. The timing ramp equation is:

$$V_T = (V_{cc} - V_{D1}) \quad (1-e^{-t/RC}) + V_{D1}$$

where V_{CE} of Q10 is neglected. With the resistance ratio equal to 0.32, substituting for V_T yields

$$(V_{cc}-V_D)\ (0.32) + V_{BE(Q11)} = (V_{cc}-V_D)\ (1-e^{-t/RC}) + V_D\ .$$

With equal diode voltages, the output period will be determined only by the resistance ratio and the timing components R_X-C_X. The data sheet for the 9601 (16) indicates the following relation for the pulse width T:

$$T = 0.32\ R_X C_X\ (1 + \frac{0.7}{R_X})$$

where R_X is in KΩ, C_X is in pF and T is in nanoseconds.

When the trigger level V_T is reached, Q11 begins to turn ON and Q3 cuts OFF, driving the output stage ON. Because R_X in parallel with R_{13} cannot maintain at the top of R_{16} the voltage level that was previously maintained by R_{13} in parallel with R_{15}, the turnover action is regenerating with C_X discharging into the base of Q2, further speeding the action. The impedances connected to the monostable are large enough to prevent false triggering from ground or power-supply noise.

In the output circuitry Q13, Q14, Q15 and Q16 form a four-diode hold-off for the true output. Q12 also functions as a current-gain stage. The Q14 emitter and D7 connect directly to the differentiator output to substantially reduce delay in the circuit. The Q13 base-stored charge pulls the charge out of the base of Q14 (phase splitter). In the comparator, R_{14}, bypassing D6, ensures sufficient output drive at low voltage and temperature. The complemented output is obtained from a TTL inverter with active pullup and is driven by the true output.

B. A 710 HIGH-SPEED DIFFERENTIAL COMPARATOR; FAIRCHILD LINEAR INTEGRATED CIRCUIT (11, 14, 20).

A differential voltage comparator is a high-gain, differential-input, single-ended output amplifier. The function of the device is to compare a signal voltage on one input with a reference voltage on the other input, and produce a logical "ONE" or "ZERO" at the output, dependent upon which of the two inputs was higher.

The schematic diagram of the circuit is shown in Figure A-3. The input stage, formed by Q1 and Q2, is used for low offset. Q3 and Q4 are identical transistors, with Q3 providing balanced biasing for the second-stage amplifier, Q4. The bases of Q3 and Q4 are fed from a common voltage point, the emitter of Q5, through resistors R_1 and R_2. Q5 keeps the input-stage collector current out of the resistor R_4. Under balanced conditions, the single-ended output of Q4 is insensitive to changes in positive supply voltage.

In the output stage, Q6 is connected as a diode to limit the positive output swing. This increases the speed as well as providing compatibility with certain integrated-circuit logic families. An emitter follower, Q7, is used at the output of Q4 to give a high output-current capability. A Zener diode, D1, in the second-stage transistor emitters provides a large input voltage range. D2, an identical Zener diode in the output emitter follower, level shifts the output back to a level compatible with logic circuits.

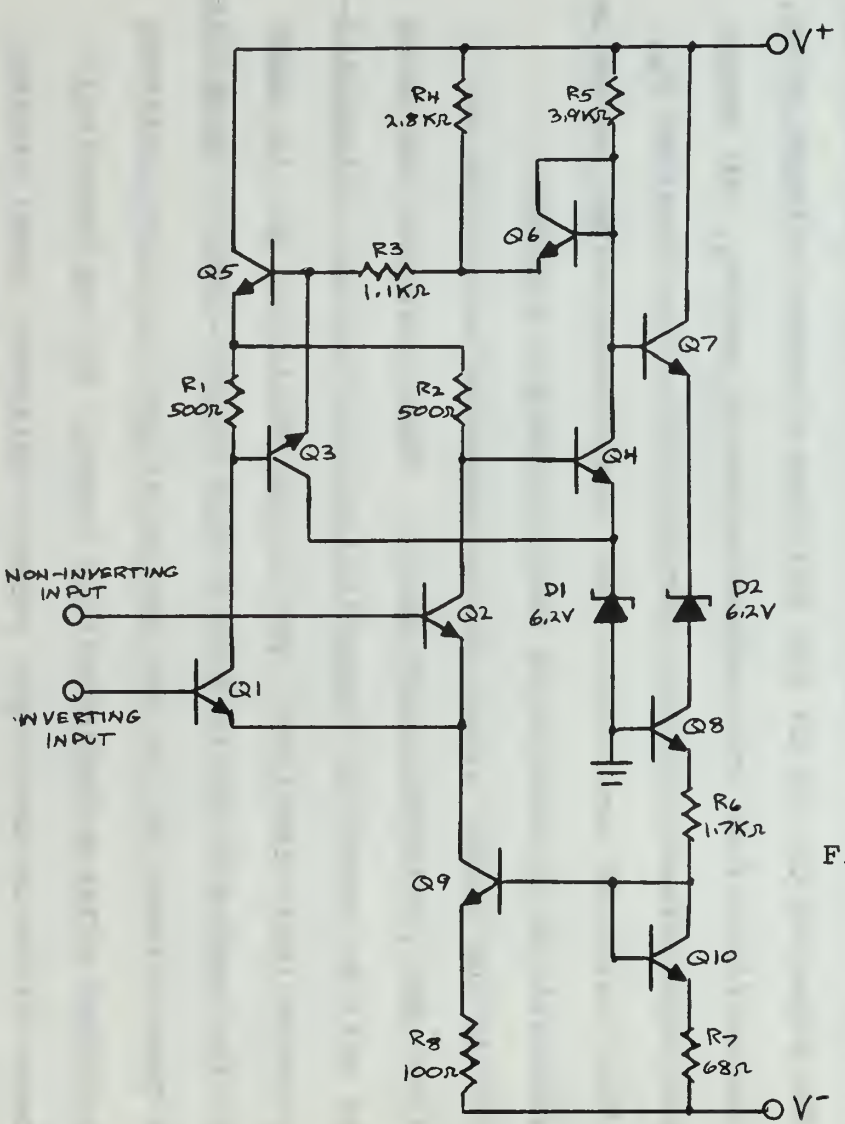


Figure A-3: Schematic Diagram of the μA 710 High-Speed Differential Comparator

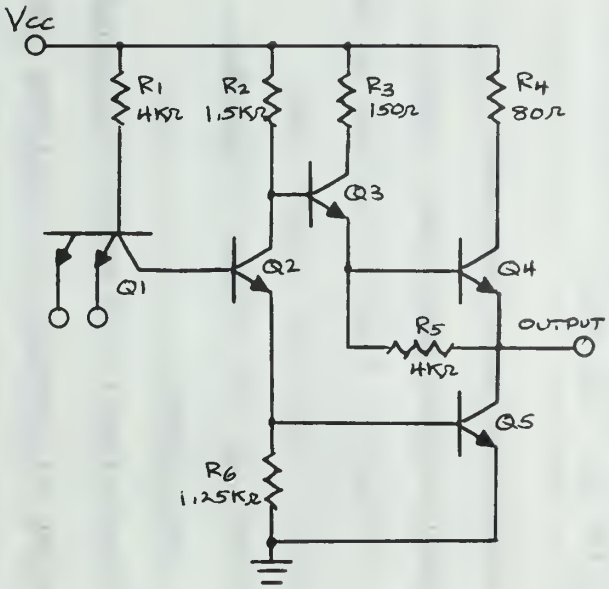


Figure A-4: Basic TTμL 9002 Two-Input Gate Circuit

Q8 isolates the output from the diode-compensated bias divider for the input-stage current source.

The input-stage emitters are supplied from the current source, Q9. With the diode-connected transistor, Q10, used to compensate for the emitter-base voltage of Q9, the current source can operate with a small voltage drop across its emitter resistor, R_8. This gives a large input-voltage limit.

C. 9002 QUAD TWO-INPUT GATE; FAIRCHILD TRANSISTOR - TRANSISTOR MICROLOGIC CIRCUIT (12, 13).

The 9002 Quad Two-Input Gate is an integrated circuit consisting of four independent gates, each with two inputs. Each gate is a high-level positive NAND gate capable of driving high-capacitance and high fan-out loads. They are designed for compatibility with Diode Transistors Micrologic (DTμL) elements. Figure A-4 depicts the basic gate circuit of the TTμL 9002.

D. A 741 HIGH-PERFORMANCE OPERATIONAL AMPLIFIER; FAIRCHILD LINEAR INTEGRATED CIRCUIT (15, 18, 19).

The μA 741 is a monolithic operational amplifier designed for high performance and ease of application. The circuit incorporates a unity-gain frequency-compensation network, thus eliminating the need for external components

which were required with the first-generation μA709 operational amplifier.

The circuit is essentially a two-stage amplifier comprising a high-gain differential input stage followed by a high-gain driver with a class-AB output. The schematic diagram is depicted in Figure A-5.

Since high-Beta PNP transistors involve costly additional processing steps, the input circuit of the 741 uses a combination of high-Beta NPN and low-Beta PNP transistors to achieve low input-bias currents. The device is able to withstand ±30 volts differential input signals without breakdown of the base-emitter junction of Q1 or Q2. This is due to the larger emitter-base breakdown voltage for a lateral PNP as compared to that of an NPN.

Using the high output resistance of Q5 and Q6 as loads, the stage will produce high gain. The bias network formed by Q8, Q9 and Q10 provided the operating collector current of the input stage.

The capacitor C_1 forms a portion of the frequency-compensation network. The presence of a 30-pF capacitor on the chip with stable, close tolerances, was a significant advance in linear circuit processing.

A Darlington driver (basically Q16 and Q17) is used to avoid loading the first stage. The output stage uses a conventional complementary symmetry design. A quiescent

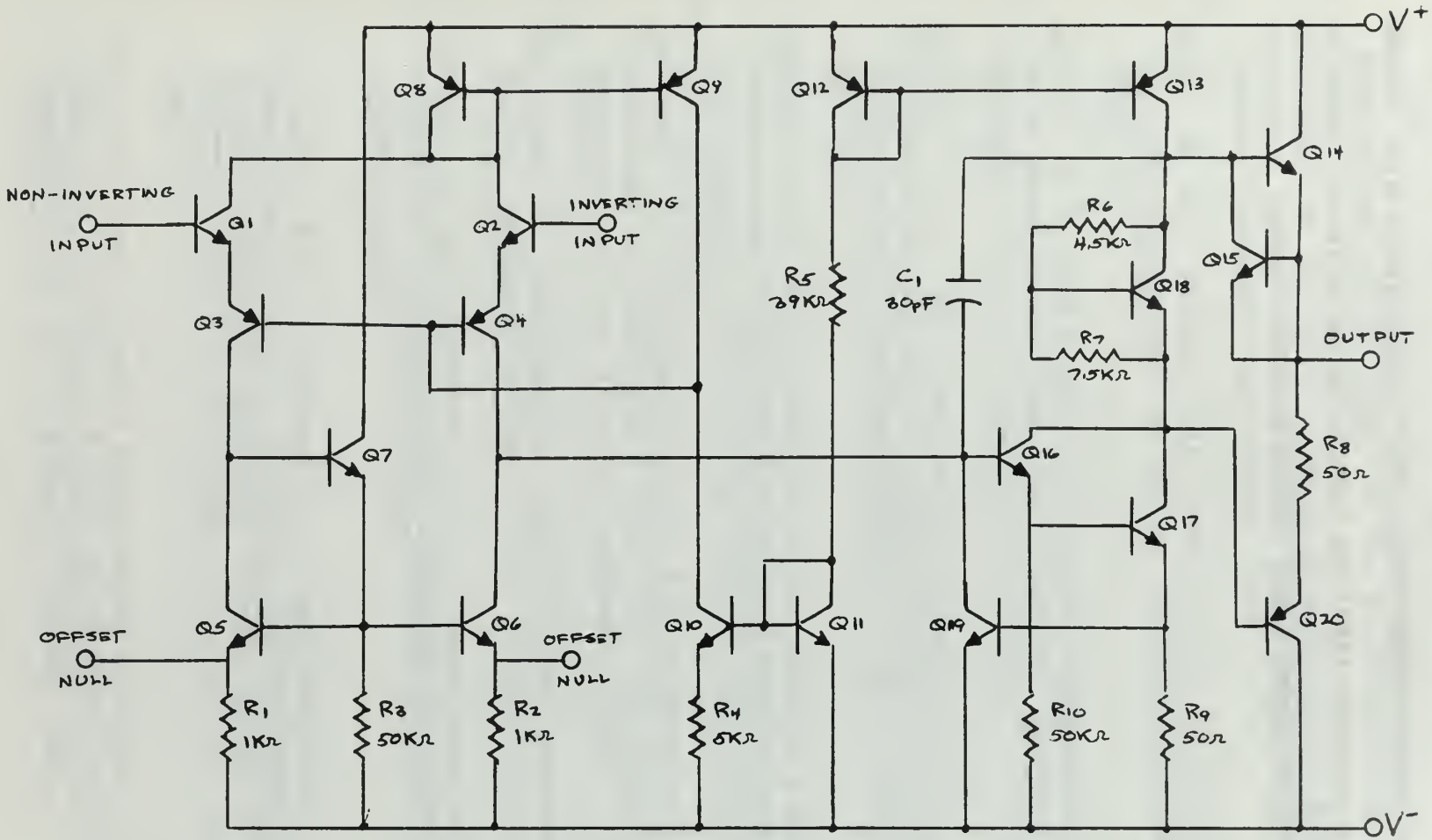


Figure A-5: Schematic Diagram of the μA 741 High-Performance Operational Amplifier

bias current of about 60 μA through Q14 and Q20 eliminates any crossover distortion. The output stage also incorporates current-limiting circuitry to prevent excessive chip dissipation under short-circuit conditions.

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13. ABSTRACT

Pulse-modulation and integrated circuits, respectively, are the most recent major advances in the communications field and in electronic devices. The evolutionary development of one pulse-modulation technique, Delta Modulation, is examined in this thesis to determine the feasibility of extending its evolution to the inclusion of integrated circuits in its design. An experimental circuit, demonstrating this feasibility, is described and evaluated.

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
DELTA MODULATION						
INTEGRATED CIRCUIT						
INTEGRATED-CIRCUIT DELTA-MODULATION SYSTEM						
PULSE MODULATION						